PUSHING CMOS LIMITS FOR BROADBAND SIGNAL GENERATION AT MILLIMETER WAVE AND TERAHERTZ FREQUENCIES

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PUSHING CMOS LIMITS FOR BROADBAND SIGNAL GENERATION AT MILLIMETER WAVE AND TERAHERTZ FREQUENCIES

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Applications at frequencies ranging from sub-millimeter wave to THz (100GHz to 1THz) are gaining a lot of attention. High frequencies can be employed for sub-millimeter wave astronomy in the field of heterodyne spectroscopy, sensing and imaging for security and detection of concealed weapons and explosives. Because of the lower f_{max} of solid state active devices, scaling of low frequency electronics to high frequencies is very challenging. At the same time, it is very difficult to make efficient semiconductor lasers of wavelength lower than 30μm. Because of the dearth of high power and tunable sources at these frequencies, this part of spectrum is usually called "THz gap".

Over the past few years, tremendous effort has been made towards solid-state THz sources. The world is looking for CMOS solutions to this problem because of the low cost of fabrication and ease of integration. The challenge in CMOS is low quality factor of passives, lossy substrate and limited f_{max} of the transistors which is still under $300GHz$. To overcome these challenges two kinds of signal generation techniques at high frequencies are employed. 1) Frequency multiplication. 2) Collecting higher order harmonics from the fundamental VCO. Owing to these two signal generation technique, my research has been focused on both frequency multipliers and oscillators.

In recent literature, few high frequency oscillators works are reported. However the major challenge has been to achieve high power and high tunability both at the same time with decent DC-RF efficiency. Since higher harmonic power is strongly dependent on the fundamental power, I have decomposed this problem in to two parts. 1) Coming up

with a VCO topology that is capable of providing high tunability along with high power and DC-RF efficiency at fundamental frequency. 2) Efficiently extracting harmonics from the VCO without affecting operation at fundamental frequency. First two chapters discusses our work on these two parts.

In chapter 1, a loop of unidirectionally coupled oscillators to demonstrate high tuning range and output power is proposed. To achieve large tuning range, two different tuning mechanisms are simultaneously exploited. First each core oscillator is tuned using a variable capacitor. Next, by controlling the phase/delay between the coupled oscillators, the entire loop dynamics and hence its frequency is tuned. In this work, we analyze a loop of "n" coupled oscillators using Adler's equation and derive the expression for the maximum tuning range. Perturbation analysis is used to study the stability conditions of the loop of coupled system. Activity condition from two port theory is also employed to squeeze maximum power out of active devices. The proposed system is designed and implemented using four coupled Colpitts VCOs in a 65nm bulk CMOS process. The VCO achieves continuous tuning range of 9.5% at the center frequency of 105GHz with the peak output power of 2.8mW. The circuit consumes 54mW from a 1.2V supply. To the best of our knowledge, this VCO has the highest output power and tuning range among all the CMOS oscillators at or above 100GHz.

In chapter 2, we employ a loop of unidirectionally coupled harmonic oscillators. To accomplish large tunability, tuning via variable capacitance and via variable coupling delay between oscillators are simultaneously exploited. A large fundamental power to produce high second harmonic is generated using activity condition of the transistors derived through two port theory. All the undesired leakage of second harmonic current is blocked thus extracting maximum power at the output. A passive coupling between VCOs is employed to enhance DC-RF efficiency. Each oscillator is realized with modified self-feeding Colpitts architecture. To demonstrate our methodology, a two stage

and an eight stage second harmonic VCOs are designed and fabricated in a 65nm bulk CMOS process. The 2-stage and 8-stage VCO achieves maximum power of -2.1dBm and 3.7dBm with DC-RF efficiency of 0.9% and 0.8%. Both VCO achieve tuning range of 8.6% at 260GHz. The two stage and eight stage VCO consume 198mA and 49mA from a 1.2V DC supply. To the best of our knowledge, these VCOs have the highest output power, tuning range and DC-RF efficiency among all the CMOS oscillators at or above 0.25THz.

Chapter 3 and 4 deal with the frequency multipliers. Our research on frequency multipliers is focused on passive nonlinear transmission line (NLTL) based structures.

In chapter 3, we develop a methodology of phase matching using bandgap transmission lines between the fundamental input and higher harmonics . We demonstrate the proposed methodology using a board level prototype that produces second harmonic with conversion loss of 5.5dB.

Chapter 4 extends the concept proposed in chapter 3 for implementation in CMOS. Two methodologies are developed to go beyond the limitations of multipliers: i) we used bandgap structure to resolve dispersion which is inherently present in any discrete wave propagating structure. ii) in order to enhance conversion loss performance and relax input power requirement, we employ a resonator approach in combination with active loading. We build two prototypes: a 20GHz frequency doubler is implemented in a 65nm process as a proof of concept, second to show the feasibility of our approach near f_{max}, a 100GHz frequency tripler is implemented in a 130nm process. The achieved conversion loss is 3.5dB for doubler and 12.2dB in case of tripler. Both structures take single ended input and generate differential output. The frequency tripler can generate maximum power better than -1.5dBm. The relative bandwidth of doubler and tripler is about 23% and 12.3%. The frequency tripler outperforms any previously reported work in terms of output power and 3dB bandwidth at the same technology node.

BIOGRAPHICAL SKETCH

Muhammad Adnan comes from a small and beautiful town named Wah Cantt in Pakistan. He completed his B.E. in Computer Engineering from National University of Sciences and Technology (NUST), Pakistan in 2005. He is currently working towards his PhD degree in the School of Electrical & Computer Engineering (ECE), Cornell University. His current research is focused on efficient signal generation at millimeter wave and terahertz frequencies.

From 2005-2007, he was with Center for Advanced Research in Engineering (CARE), Pakistan. In CARE, he worked on several encoding/decoding algorithms, hardware design of high speed digital receivers, development of an area-optimized algorithm for voice activity detection in T3/E3 stream channels, and later, as an independent assignment, hardware/software implementation of a data communication protocol. He spent the summers of 2012 with Qualcomm Atheros working on the design of low-loss passive phase shifter for a 60GHz phase array transceiver.

Mr. Adnan was recipient of the President Gold medal and Rector Gold medal in 2005, Irwin and Jacobs fellowship in the spring of 2012 and Analog Design fellowship during 2012-2013.

To my parents

for their unconditional love, immense support and help in every phase of my life.

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A 105GHZ VCO WITH 9.5% TUNING RANGE AND 2.8MW PEAK OUTPUT POWER IN A 65NM BULK CMOS PROCESS

1.1 Introduction

High frequencies ranging from sub-millimeter wave to THz (100GHz to 1THz) presents themselves with number of applications [1] [2]. Most notable of them are sub-millimeter wave astronomy in the field of heterodyne spectroscopy [3] [4], sensing and imaging for environment and security purpose [5] , detection [6] [7] [8] and communication [9] [10]. Almost all the THz applications need a high power tunable signal source. Scaling of low frequency electronics to high frequencies is very challenging. At the same it is very difficult to make semiconductor lasers of wavelength lower than 30μm [11]. Because of dearth of high power, efficient and tunable sources at these frequencies, this part of spectrum is usually called “THz gap”.

Generation of high frequencies in CMOS is gaining a lot of attention because of the low cost of fabrication and high yield. Despite fast scaling and process refinements of CMOS technology, f_{max} of active devices is still less than 300GHz which gets even lower in the presence of parasitics from interconnects. Hence in CMOS, THz sources are usually accomplished by harmonic generation. Either higher order harmonics are collected from a fundamental oscillator or separate frequency multipliers are employed. For an integrated solution of wide-band signal generation, both approaches require high power and tunable fundamental oscillators at mm-wave frequencies (~100GHz).

Achieving both high power and high tunability at the same time in CMOS mm-wave oscillators is not trivial. The low frequency oscillator design methodologies cannot be

applied directly at the mm-wave frequencies because in formers case, performance is limited by the quality factor of inductor however in later, varactor limits the performance in terms of output power, tunability as well as phase noise. The output power is strongly affected by the low quality factor of varactor employed in the LC tank for tuning purpose. The typical value of quality factor of varactor is less than 10 at 100GHz. The tuning capability of varactor is severely effected because at these frequencies device parasitics become comparable with the size of varactor. Also in most cases, varactor comes in parallel with the device parasitic capacitances, hence it lowers the maximum oscillation frequency. The existing techniques of magnetic tuning [12] and resonant mode switching [13] cannot be applied at mm-wave frequencies as these schemes rely on switches either inside the tank or in the G_m network which adds extra loss in "ON" state and additional parasitics in "OFF" state.

In this work, we combine two mechanisms simultaneously: tuning via variable capacitance and tuning via variable delay of coupled oscillator [15][14]. To accomplish both, a loop of unidirectional coupled oscillator is employed. Besides providing an extra dimension of tuning, coupling also enhances output power as well as phase noise. We study the dynamics of loop of coupled system using Adler's equation [16]. From the phase dynamics, we derive the maximum tuning range of such coupled system. Stability of the system is studied using perturbation analysis. Circuit level implementation of the proposed methodology is realized through a loop of coupled Colpitts oscillators. The proposed circuit is implemented without any explicit phase shifters. To further enhance the power, two port theory is used to study the activity condition of active devices. The results of the activity condition are used to maximize the power produced by transistors. A prototype of VCO is build at 105GHz in a 65nm CMOS process. The VCO achieves continuos tuning range of 9.5% with maximum output power of 4.5dBm and DC-RF efficiency of 5.5%. The circuit consumes 58mW from 1.2V DC supply. These results

outperform any previously reported CMOS VCO at or above 100GHz in terms of tuning range, output power and DC-RF efficiency.

The rest of the paper is organized as follows: Section II describes the discusses the employed tuning mechanism along with the analytical treatment of phase dynamics as well as stability analysis. Section III presents realization of the proposed system using Colpitts oscillators. Section IV provides design and simulation of the proposed methodology in a 65nm CMOS process as well as the activity condition of the two port network to squeeze maximum power out of the active devices. Section V contains measurement results and comparison with the state of art followed by conclusion in Section VI.

1.2 Tuning Mechanisms

Adler presented dynamics of a system of coupled electrical oscillators in the context of injection locking [16]. When a free running oscillator at ω_o is injected with a signal from another oscillator at ω, under certain conditions the first oscillator locks to second oscillator at ω. This locking results in a phase difference ($\Delta\phi$) between two oscillators which is proportional to the frequency difference ($\Delta\omega = \omega - \omega_o$) given by

$$\Delta\phi = sin^{-1}\left(2Q\frac{I_{core}}{I_{inj}}\frac{\Delta\omega}{\omega_o}\right) \tag{1.1}$$

where Q is the quality factor of the resonator and I_{core} and I_{inj} are the currents inside core and injected from the outside, respectively. Conversely, the oscillation frequency of two mutually coupled oscillators can be controlled by enforcing a certain phase shift between them [15].

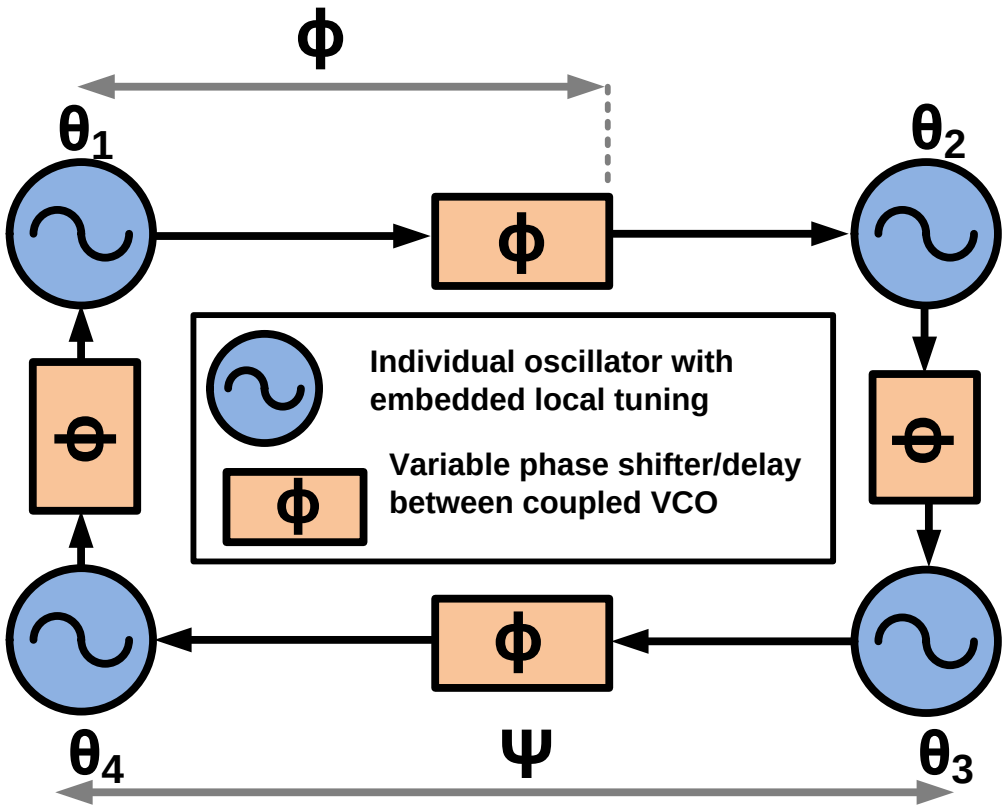

Figure 1.1: A loop of coupled oscillators having local & global tuning

In this work, we employ a system of coupled oscillators as shown in Fig. 1.1. Two kinds of tuning phenomenon occur in such a system: local tuning and global tuning. Local tuning is implemented at the level of individual oscillators using varactors inside each core. On the other hand, global tuning is achieved at the system level where frequency variation is performed by changing the coupling between core oscillators [15]. In this work, we design the system in such a way that the overall tuning range is the addition of both approaches.

1.2.1 Phase dynamics and stability analysis of a single loop of coupled oscillators

If ϕ is the rotating phase of i^{th} oscillator in the loop and ω_o is its free running frequency then from the theory of injection locking the instantaneous frequency is given by

$$\dot{\theta}_i = \omega_o + K sin(\phi - (\theta_i - \theta_{i-1})) \tag{1.2}$$

where $K = \frac{I_{inj}}{I_{core}} \frac{\omega_o}{2Q}$ is the coupling factor and ϕ is the phase shift resulting from the phase shifter in Fig. 1.1.

Now we assume each oscillator consists of an LC tank and has a varactor that results in local tuning. If ΔC is the change in capacitance then (1.2) can be transformed in to

$$\dot{\theta}_i = \omega_o \left(1 + \frac{\Delta C}{2C_o}\right) + K_s sin(\phi - (\theta_i - \theta_{i-1})) \tag{1.3}$$

where

$$K_s = \left(1 + \frac{\Delta C}{C_o}\right) \frac{I_{inj}}{I_{core}} \frac{\omega_o}{2Q}$$

is the coupling factor of the system.

Assuming ψ is the instantaneous phase shift between two adjacent oscillators

$$\begin{aligned} \psi_i &= \theta_i - \theta_{i-1} \\ \dot{\psi}_i &= K_s sin(\phi - \psi_i) - K_s sin(\phi - \psi_{i-1}). \end{aligned} \tag{1.4}$$

For steady state solution $\dot{\psi}_i = 0$. Furthermore, closed loop also imposes another boundary condition i.e. $\sum_i \psi_i = 2k\pi$ where k is an integer that must be greater than equal

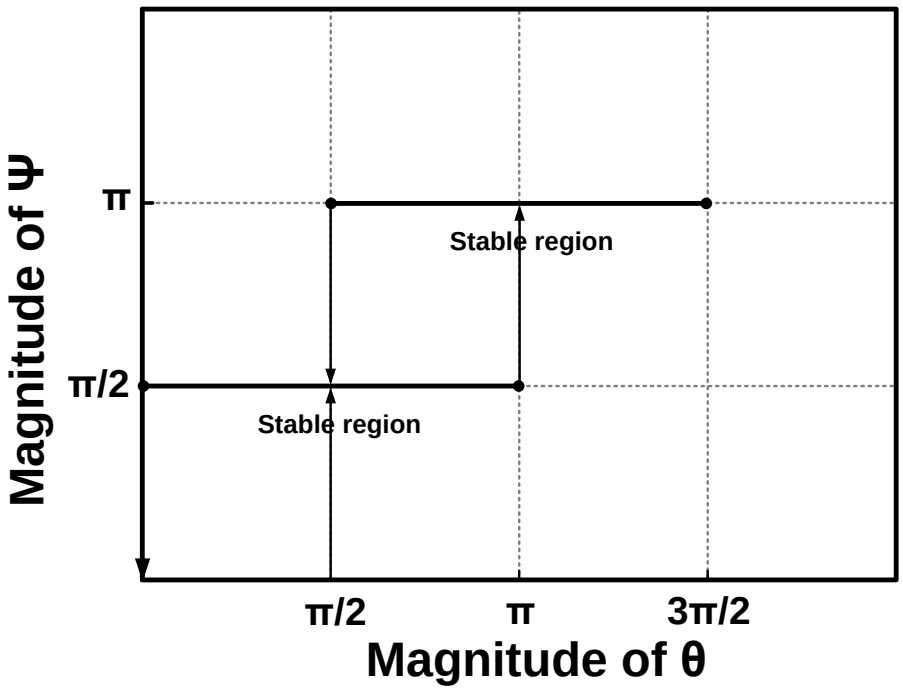

Figure 1.2: Stable regions for different modes of coupled oscillators.

to 1. It has been proved using perturbation analysis in [14] that any phase dynamics of form (1.4) is stable if

$$K_s = (1 + \frac{\Delta C}{C_o})\frac{I_{inj}}{I_{core}}\frac{\omega_o}{2Q} \geq 0 \tag{1.5}$$

and

$$\psi + \pi/2 \geq \phi \geq \psi - \pi/2. \tag{1.6}$$

The condition presented in (1.5) is satisfied in electronic oscillators as $\frac{\Delta C}{C_o}$ is usually greater than -1. To understand (1.6), please consider Fig. 1.2 where stable regions for two modes of a coupled system are marked using (1.6).

1.2.2 Phase dynamics and stability analysis of a nested loop of coupled oscillators

We can extend above analysis for the nested loop of coupled oscillators as shown in Fig. 1.3. Outer loop in Fig. 1.3 consists of a system of coupled oscillators similar to Fig. 1.2. Assuming $A = 1 + \frac{\Delta C}{2C_o}$, $K_t = A\frac{I_{inj}}{I_{core}}\frac{\omega_o}{2Q}$ and $K_s = \frac{I_{injn}}{I_{coren}}\frac{1}{2Q_n}$ where Q and Q_n are the quality factor internal loop and outer loop of coupled oscillators. Similary, I_{injn} and I_{coren} are the injected power and power inside the internal loop.

$$\dot{\theta}_i = \omega_o.A + K_t sin(\phi - (\theta_i - \theta_{i-1})) + K_n\left(A\omega_o + K_t sin(\phi - (\theta_i - \theta_{i-1}))\right) sin(\phi_n - (\theta_{ni} - \theta_{n(i-1)})) \quad (1.7)$$

Such a system has two kinds of phase dynamics: one in term of θ and other in terms of θ_n. We would consider one at a time assuming other as a constant to simplify the analysis. Performing the similar kind of analysis as in case of single loop leads to following stability conditions.

$$\begin{aligned} (1 + \frac{\Delta C}{C_o})\frac{I_{inj}}{I_{core}}\frac{\omega_o}{2Q} &\geq 0 \\ \frac{I_{injc}}{I_{coref}}\frac{1}{2Q_f} &\leq 1 \end{aligned} \quad (1.8)$$

and

$$\begin{aligned} \psi + \pi/2 \geq \quad \phi \quad &\geq \psi - \pi/2. \\ \psi_n + \pi/2 \geq \quad \phi_n \quad &\geq \psi_n - \pi/2. \end{aligned} \quad (1.9)$$

1.2.3 Maximum Tuning Range

Now we summarize the maximum tuning range we can achieve for different methodologies. If the oscillator has only capacitive tuning the maximum tuning range is given

by

$$\frac{\Delta\omega_{max}}{\omega_o} = \frac{\Delta C}{C_o} \tag{1.10}$$

If we employ only global tuning, then from (1.2), we can find the frequency in locked state as

$$\omega = \omega_o + K sin(\phi - (\theta_i - \theta_{i-1})) . \tag{1.11}$$

The maximum tuning range can occur when the argument of sine in (1.2) changes from $-\pi/2$ to $\pi/2$, hence

$$\left.\frac{\Delta\omega_{max}}{\omega_o}\right|_{global} = \frac{I_{inj}}{I_{core}}\frac{1}{Q}. \tag{1.12}$$

Similarly, frequency in steady state for both both local(capacitive) and global tuning can be written using (1.3) as

$$\omega = \omega_o\left(1 + \frac{\Delta C}{2C_o}\right) + K_s sin(\phi - (\theta_i - \theta_{i-1})) \tag{1.13}$$

It is noteworthy that (1.13) shows the relationship between the frequency of the coupled oscillators and the phase shift between them. In particular, as the phase shift, ϕ, increases (or the delay between oscillators decreases) the frequency of the system, ω, increases and vice versa. The maximum tuning range from (1.13) is

$$\left.\frac{\Delta\omega_{max}}{\omega_o}\right|_{local+global} = \frac{\Delta C_{max}}{C_o} + \frac{I_{inj}}{I_{core}}\frac{1}{Q}, \tag{1.14}$$

which comes out to be the sum of (1.12) and (1.10).

For locked state, maximum tuning range can also be calculated for nested loop case from (1.7):

$$\left.\frac{\Delta\omega_{max}}{\omega_o}\right|_{nested} = \frac{\Delta C}{C_o} + \left(\frac{I_{inj}}{I_{core}}\frac{1}{Q} + \frac{I_{injn}}{I_{coren}}\frac{1}{Q_n} + \frac{I_{injn}}{Q_n I_{coren}}.\frac{I_{inj}}{2QI_{core}}\right).$$

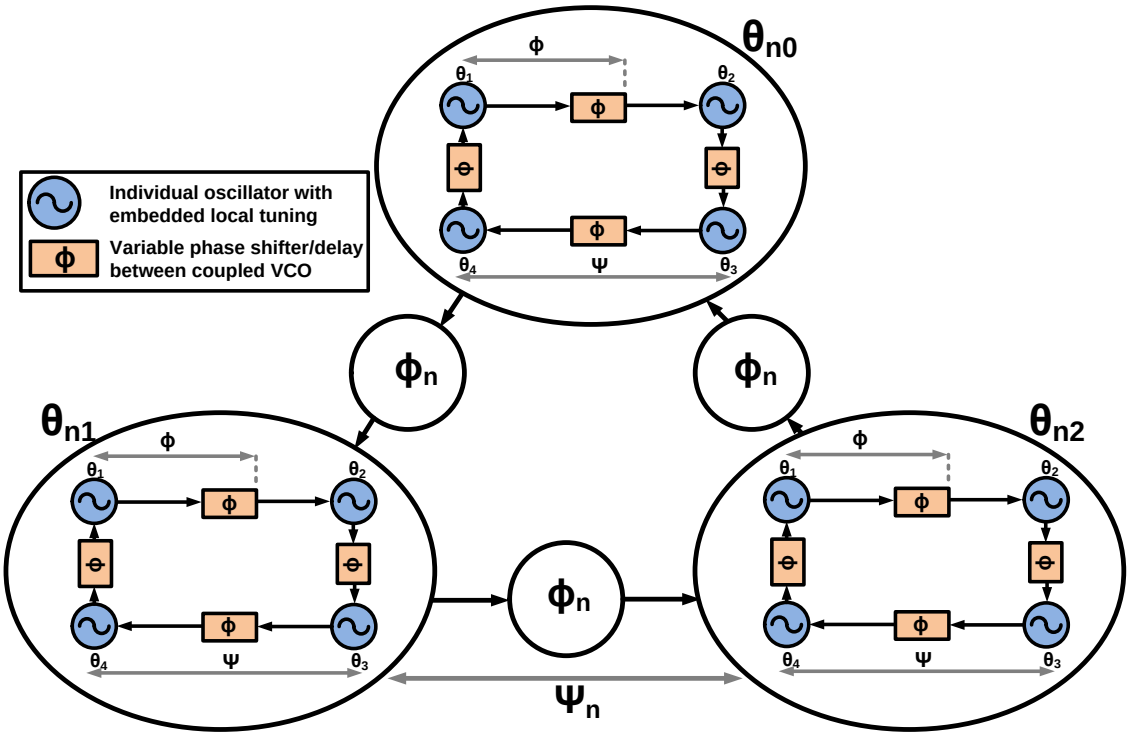

Figure 1.3: Nested loop of coupled oscillators.

Hence we propose a incremental way of pushing tuning limits of high frequency VCOs using system of coupled oscillator arranged in a loop and nested loop fashion along with capacitive tuning. In this work, we have implemented a loop of unidirectionally coupled oscillator using Colpitts VCOs to simultaneously exploit global and local tuning as described in (1.14). We do not employ explicit phase shifters in our system that significantly reduces power cosumption as well as design complexity.

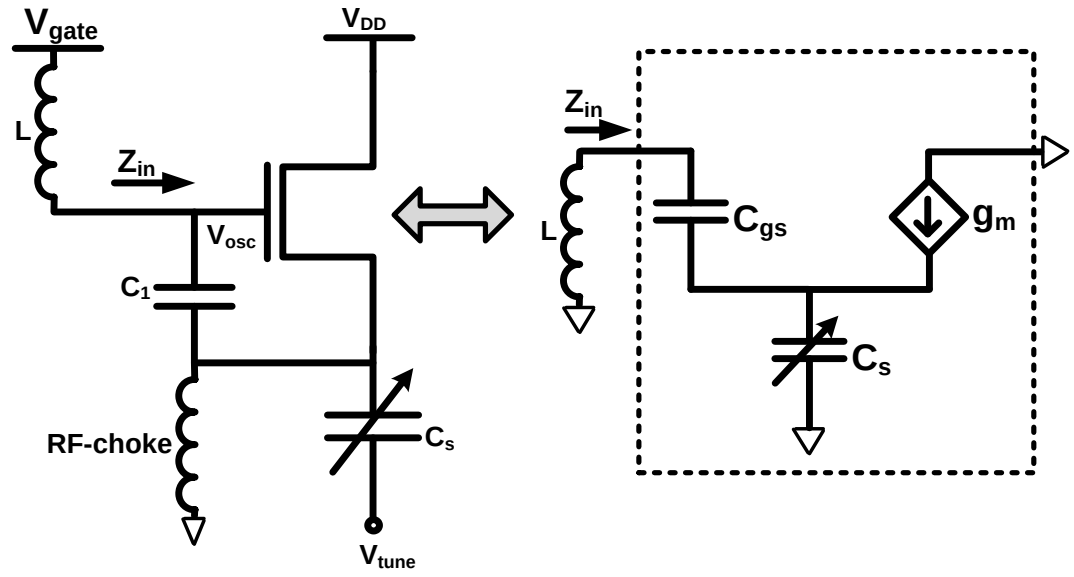

Figure 1.4: Common drain Colpitts

1.3 Circuit level realization of proposed system

The implementation of both global and local tuning in one system is challenging. We choose common drain Colpitts topology for the implementation of each oscillator of Fig. 1.1 because, as explained later, it allows us to implement global tuning without any explicit phase shifters hence resulting in a simpler implementation. Moreover, in the case of Colpitts, varactor comes in series with the parastic capacitance hence the presence of varactor does not decrease the oscillation frequency. The common drain Colpitts is shown in Fig. 1.4 with a varactor at the source of transistor. The parasitic capacitance between gate and source (C_{gs}) acts as a feedback capacitor so we can eliminate C_1. The small signal analysis yields to

$$Z_{in} = \left(\frac{1}{C_s} + \frac{1}{C_{gs}}\right)\frac{1}{j\omega} - \frac{g_m}{\omega^2 C_{gs} C_s}$$

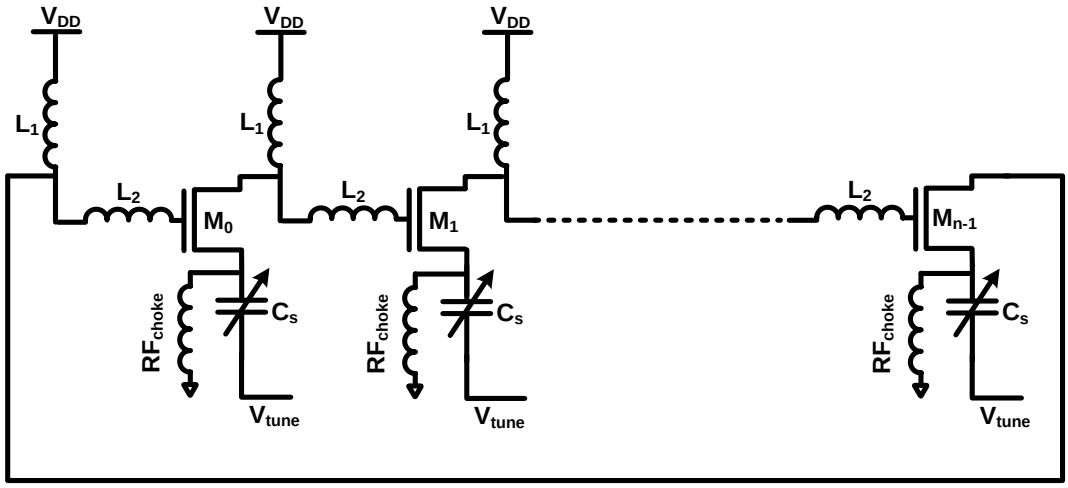

Figure 1.5: Coupling scheme of "n" Colpitts VCOs

at the gate of transistor. The above equation contains negative real impedance along with the variable imaginary part. The negative real impedance compensates for the loss of the tank.

We couple "n" Colpitts oscillator as shown in Fig. 1.5. We do not employ any explicit phase shifters. The energy from each stage is injected from the gate of transistor in to the next stage via the drain current. The varactor inside each core also varies the phase of injected current along with changing the oscillation frequency of the system.

1.3.1 Global tuning in a loop of coupled Colpitts

We look at the phase of Y_{21} of a transistor with capacitor at the source in order to understand global tuning in Fig. 1.5. A $20\mu m$ wide transistor in a 65nm CMOS process is simulated with capacitor at the source. The phase of Y_{21} is plotted at 100GHz in

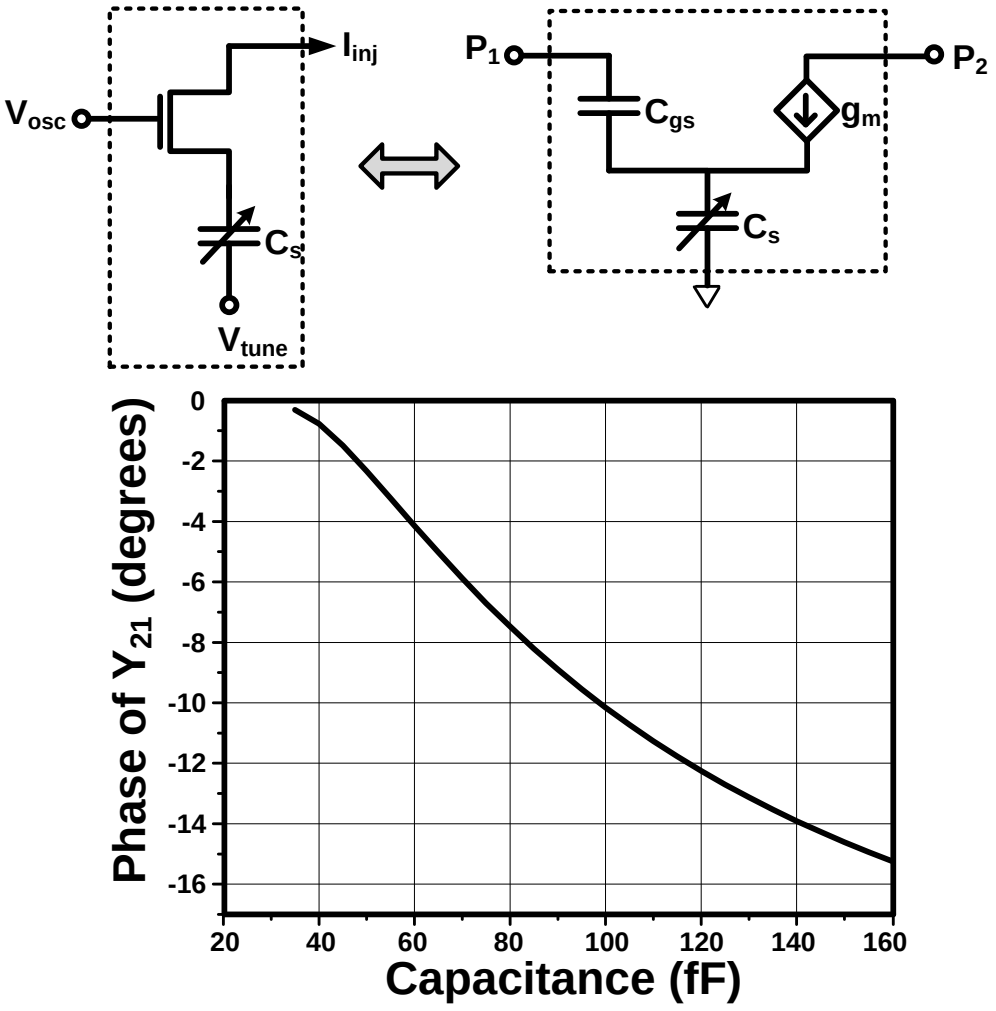

Figure 1.6: Simulated phase of Y_{21} against capacitance at 100GHz

Fig. 1.6 against capacitance at the source. Recall from the last section that phase delay corresponds to global tuning:

$$\left.\frac{\Delta\omega_{max}}{\omega_o}\right|_{global} = K sin(\theta_{delay}). \tag{1.15}$$

From Fig. 1.6, two effects happen with change in capacitance. Consider the case of decrease in capacitance: i) it increases the local frequency of each oscillator of Fig.

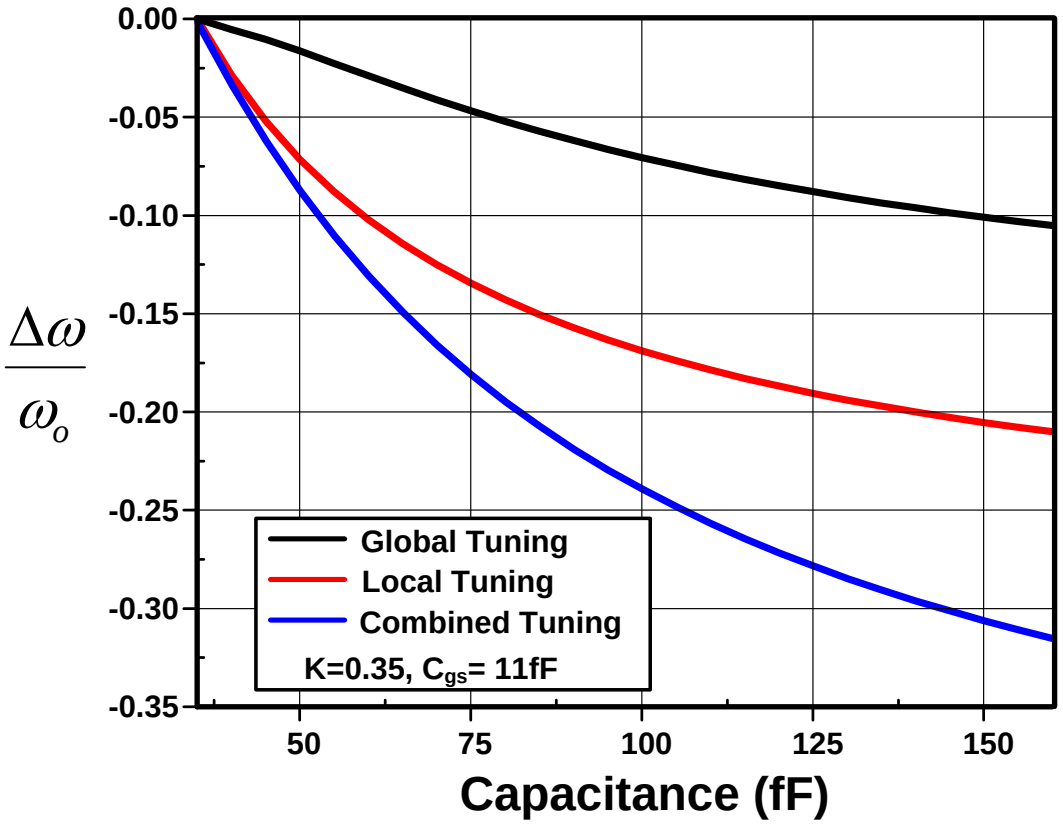

Figure 1.7: Analytical calculation of global tuning, local tuning and combination of both.

1.5. ii) it increase the phase or decreases the delay of Y_{21} from (1.15), that results in increases of frequency of coupled system even more. Both effects add constructively for the region of capacitance change shown in Fig. 1.6.

From the phase delay and capacitance change shown in Fig. 1.6, we can analytically calculate the relative change in frequency due to local tuning and global tuning. The calculated tuning range is plotted is in Fig. 1.7.

Fig. 1.7 shows that both local and global tuning works in the same direction. The

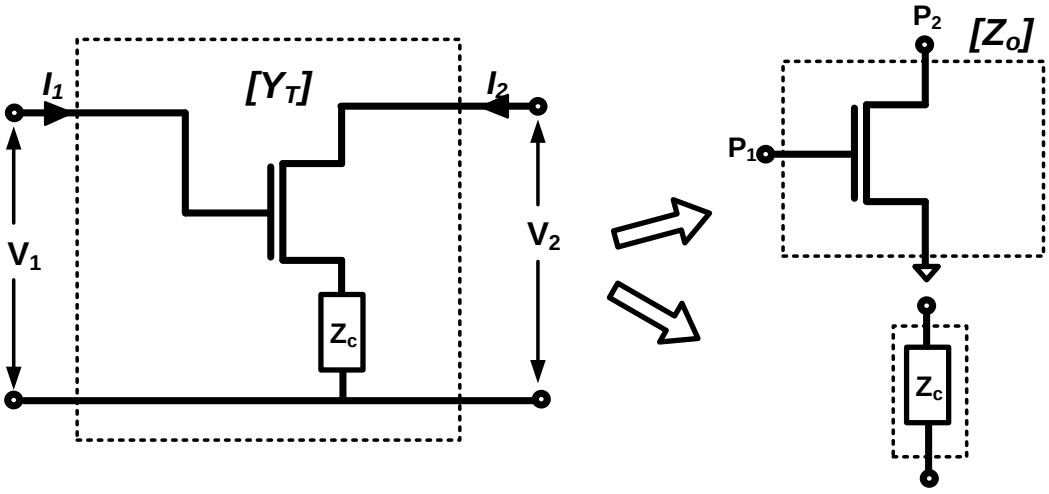

Figure 1.8: Two port network of a transistor with the capacitor at the source.

proposed topology enables the same varactor to provide both local and global tuning. Moreover coupling improves the output power as well as the phase noise.

1.3.2 Optimum phase condition to achieve maximum power

To achieve maximum power coming out of the active devices in VCO design, we look at the activity condition from the perspective of two port theory [17]. In order to derive optimum phase condition similar to [18] and [19] for the proposed VCO, we must convert the transistor with capacitor at the source in to a two port network. We can break such a series network in to two two networks as shown in Fig. 1.8.

$$\begin{aligned}\left[Z_T\right] &= \begin{bmatrix} Z_{T11} & Z_{T12} \\ Z_{T21} & Z_{T22} \end{bmatrix} \\ \left[Z_T\right] &= \left[Z_o\right] + \begin{bmatrix} Z_c & Z_c \\ Z_c & Z_c \end{bmatrix}. \end{aligned} \tag{1.16}$$

Y-parameters of the network under study can be found using

$$\left[Y_T\right] = \left[Z_T\right]^{-1}.$$

Now the power coming out of two port network shown in Fig. 1.8 can be written as

$$P_{out} = -Re(V_1 I_1^*) - Re(V_2 I_2^*)$$

We can plug in the values of I_1 and I_2 from the Y matrix.

$$\begin{aligned} I_1 &= Y_{T11} V_1 + Y_{T12} V_2 \\ I_2 &= Y_{T21} V_1 + Y_{T22} V_2. \end{aligned}$$

Assume,

$$A = \frac{V_2}{V_1}$$

and g_{ij} and b_{ij} as the real and imaginary part of Y_{Tij} then:

$$P_{out} = -g_{11}|V_1|^2 - g_{22}|V_2|^2 - |V_1||V_2|\left((g_{12} + g_{21})cos\angle A - (b_{21} - b_{12})sin\angle A\right).$$

In case of oscillators, magnitude of voltage gain A is usually unity, however phase is extremely important and is given by

$$\angle A_{opt} = \angle\left(-Y_{T21} + Y_{T12}^*\right). \tag{1.17}$$

Fig. 1.9 shows the plot of (1.17) for a transistor of size $20\mu m/60nm$ with and without presence of 75fF capacitor at the source. It is clear from the plot that optimum phase

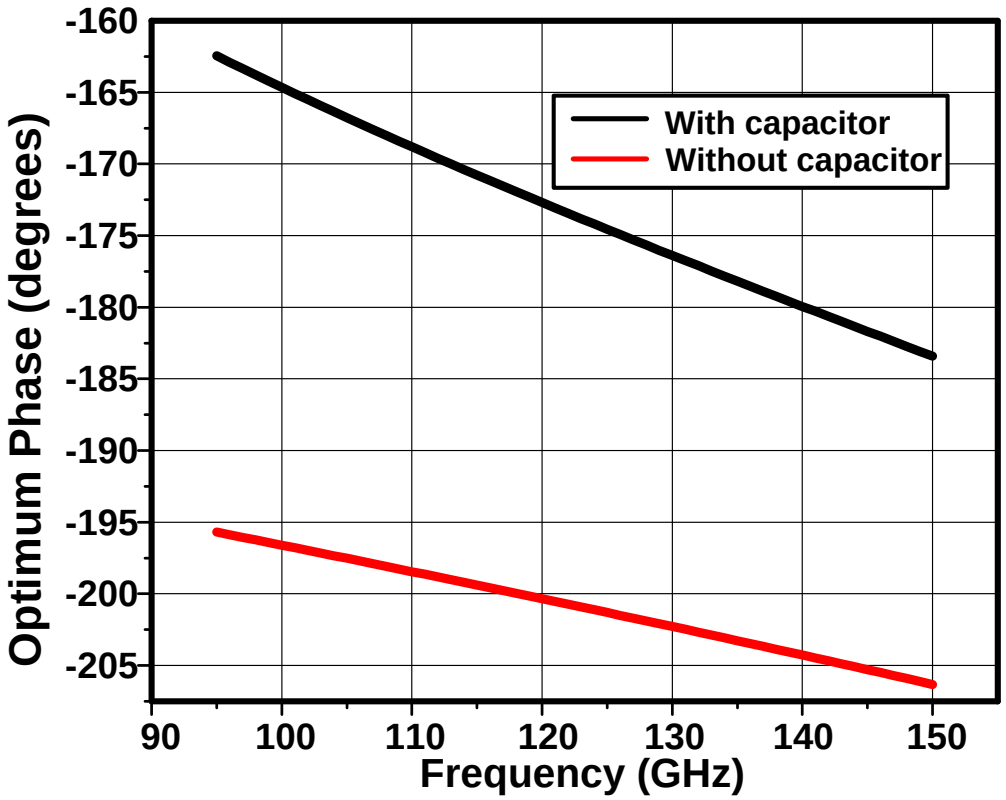

Figure 1.9: Optimum phase condition for the capacitor at the source.

condition for the cross coupled oscillator which has the phase difference of 180 degree between gate and drain is impossible to achieve without capacitive loading at the source. However, a capacitor at the source can be employed to achieve optimum phase condition as well as tuning in a cross coupled VCO.

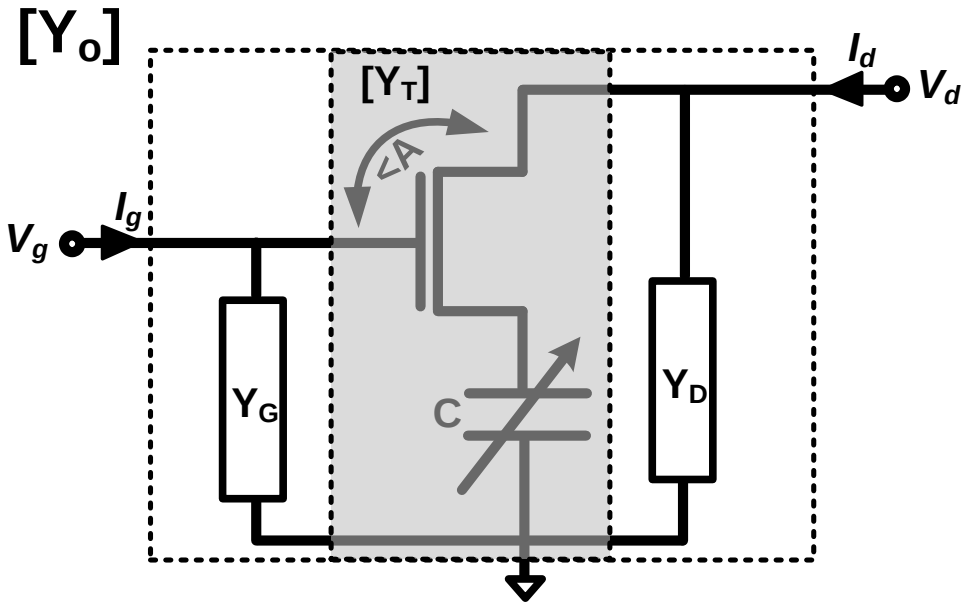

Figure 1.10: Oscillator with passives around

1.3.3 Oscillator design methodology

Having understood the optimum phase condition and tuning methodologies, next step is to design the passives of the circuit such that the oscillator oscillates at desired frequency with maximum power and required tuning range is achieved. In this section we are proposing a methodology to achieve that for our proposed design. Consider Fig. 1.10, Y_G and Y_D are admittance of everything seen by the active devices towards its gate and drain side respectively. Y_T represents the Y-matrix of transistor with the capacitor at the source. Assuming I_d and I_g are the currents entering gate and drain of the transistor then

$$\begin{bmatrix} I_d \\ I_g \end{bmatrix} = \begin{bmatrix} Y_o \end{bmatrix} \cdot \begin{bmatrix} V_d \\ V_g \end{bmatrix}$$

where Y_o can be written as

$$\begin{aligned}\left[Y_o\right] &= \left[Y_T\right] + \left[Y_{sh}\right] \\ \left[Y_{sh}\right] &= \begin{bmatrix} Y_G & 0 \\ 0 & Y_D \end{bmatrix}\end{aligned}$$

In case of oscillators, current entering and leaving must be zero then,

$$\begin{bmatrix} I_d \\ I_g \end{bmatrix} = \left[Y_o\right] . \begin{bmatrix} V_d \\ V_g \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}.$$

If A_r and A_i are the real and imaginary part of optimal gain calculated in the last section then we can transform above equation as

$$\left[Y_o\right] . \begin{bmatrix} 1 \\ A_r + jA_i \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

Solving above equation leads to following equations for Y_D and Y_G. It must be noted that optimal phase condition is already the part of design process of Y_D and Y_G.

$$\begin{aligned} Y_G &= -Y_{T11} - A.Y_{T12} \\ Y_D &= -\frac{Y_{T21}}{A} - Y_{T22} \end{aligned} \tag{1.18}$$

Above set of equations tell us the desired values of the loading, an active device must see around it. In order to further explain the design of network between the drain of one stage to the gate of next stage, assume we desire an "n" stage oscillator with phase delay of ϕ_s across each stage. It must be noted that ϕ_s must be greater the $\angle A_{opt}$ derived in the last section. The setup shown in Fig. 1.11 is recommened to verify the design of inductors and transmission lines between drain of one stage to the gate of next stage. In the Fig. 1.11, $\phi = (n-1).\phi_s + \angle A_{opt}$ and Y_D and Y_G must be close to the values analytically calculated via (1.18).

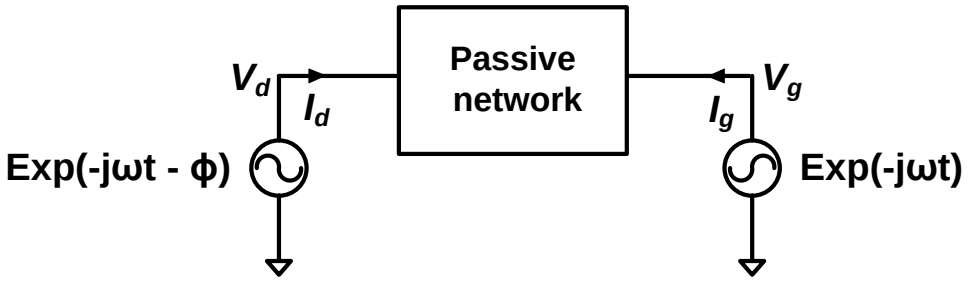

Figure 1.11: Oscillator with passives around

1.4 Implementation

Fig. 1.12 shows the schematic of four coupled Colpitts VCOs. If the RF-choke is used for biasing the source of each transistor (as in Fig 1.5.), the size of varactor comes out to be comparable with the size of C_{gs}.

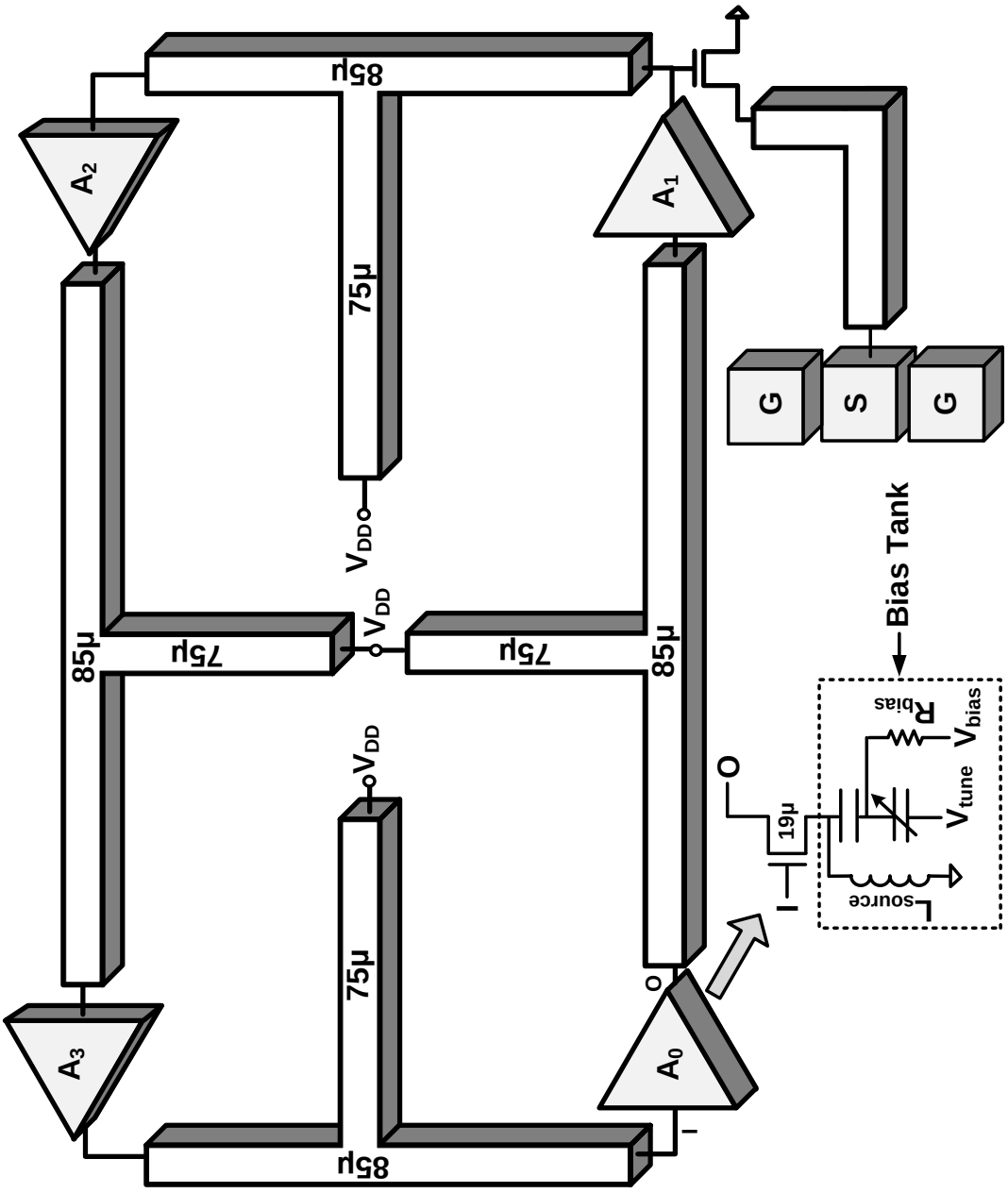

Figure 1.12: Schematic of designed VCO

The implementation of the big RF-choke inductor can potentially increase the area and make layout difficult. We resolve this problem by implementing an LC tank (referred as bias tank in Fig. 1.12) at the source of each transistor. To attain capacitive behavior at the source, resonance frequency of the "bias tank" is kept lower than the oscillation frequency of the VCO and inductance of the bias tank is selected to be around 90pH. This biasing approach gives us an extra degree of freedom in terms of varactor design. Furthermore, the varactor can be designed for the highest tunability because its capacitance does not need to be close to C_{gs}.

The proposed structure is designed at 105GHz and fabricated in a 65nm CMOS process. Each transistor is 20μm wide and consists of 20 fingers. The inductors are implemented as coplanar transmission lines with ground shielding. The transmission lines are designed to have maximum characterisctics impedance possible in this fabrication process (55-70Ω). The width of transistors are chosen to match the optimum phase condition ((1.17)) and passives are designed accordingly (1.18), hence ensuring maximum power design of the VCO. The chosen $\angle A_{opt}$ is greater than -180^o such that when passives are added the phase delay across each stage becomes equal to -180^o. Fig. 1.13 shows the calculated phase delay across gate and drain and the phase delay achieved in final design VCO for various values of control voltages and oscillation frequencies. It is evident from Fig. 1.13 that we achieve optimum phase in our design across the whole tuning range. The lengths of transmission lines employed are shown in Fig. 1.12 and their design dimensions are shown in Fig. 1.14. All the lines and interconnects are carefully simulated in Sonnet. The varactor is carefully chosen for the highest C_{max}/C_{min} ratio. The capacitance varies from 40fF to 200fF ($C_{max}/C_{min} > 3$). The chosen varactor along with its quality factor is shown in Fig. 1.15.

A coupling capacitor to bias the varactor was designed using the top two metal

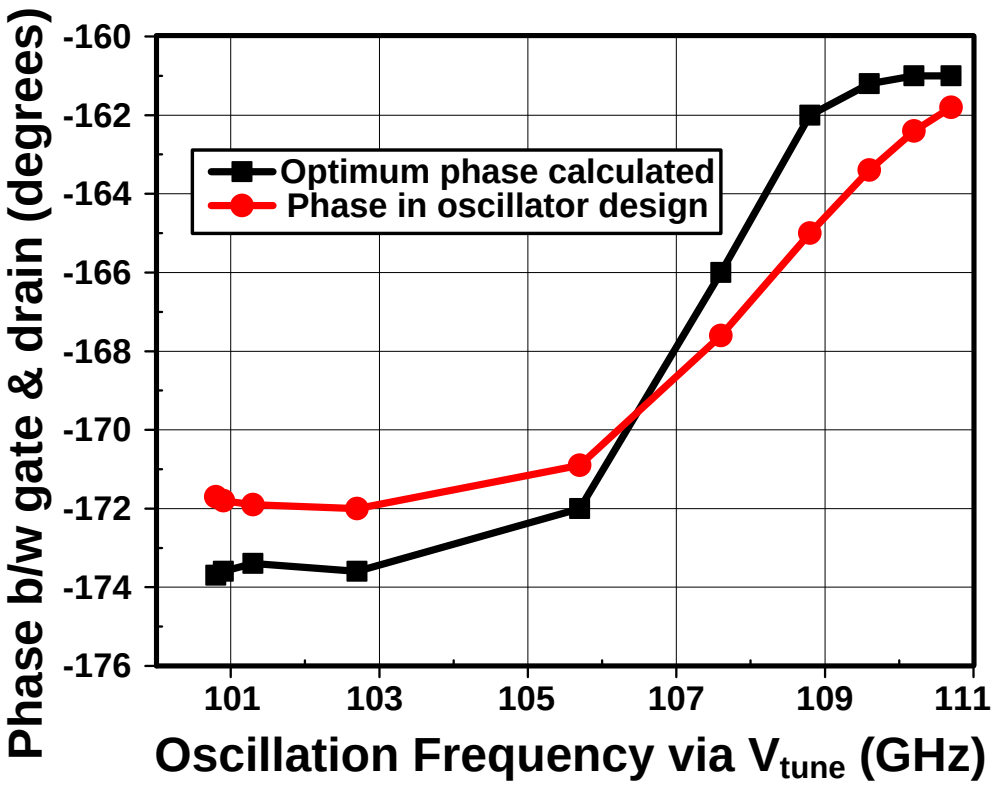

Figure 1.13: Calculated optimum phase and simulated phase in the designed prototype.

plates. We use an 18μm wide transistor as common source buffer and absorb its loading effect by adjusting the sizes of adjacent transistors. The buffer is connected to a low capacitive pad via a 50 ohms transmission line. A small 50μm x 50μm output pad is designed using the top metal layers with no ground plane. The capacitance of the pad to substrate is only 10.8fF with Q of 24 at 105GHz. The inductances of V_{DD} traces and bypass capacitors are also carefully modeled and included in the simulation. Fig. 1.16. shows the simulation results of our design. The frequency can be continuously tuned from 99GHz to 110GHz. The maximum simulated output power is 5.9dBm at 99GHz

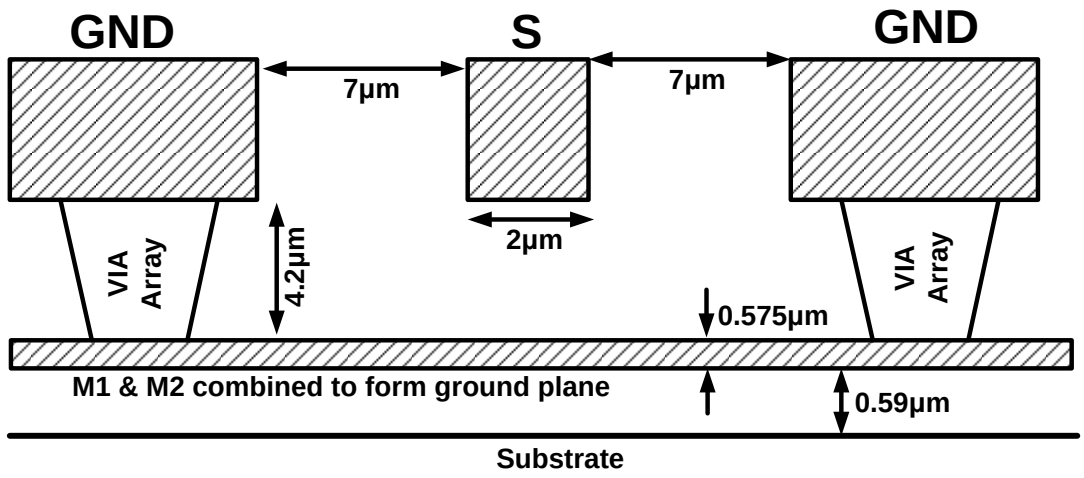

Figure 1.14: Design dimensions of transmission lines

and the power remains higher than -1dBm over all the operating range.

For testing, the chip was mounted on a PCB and all the DC voltages were wire bonded. Fig. 1.17. shows the measurement setup to determine the output power and frequency. The output is measured using a WR-08 probe by GGB with a built-in bias-T. The loss of probe is measured using a 110GHz network analyzer to be around 2.5dB at frequencies from 100GHz to 110GHz. The output buffer of oscillator is power up using the probe bias-T. The probe is directly attached to an OML harmonic mixer via a WR-08 waveguide. An external diplexer is employed to connect to a spectrum analyzer and signal generator. The conversion loss of harmonic mixer is measured at various LO powers for 8_{th}, 10_{th} and 12_{th} harmonic using a PM4 calorimeter. The loss of mixer is 37-44dB from 100-110GHz at 8_{th} harmonic of LO. The output frequency was determined by sweeping the LO at various harmonics.

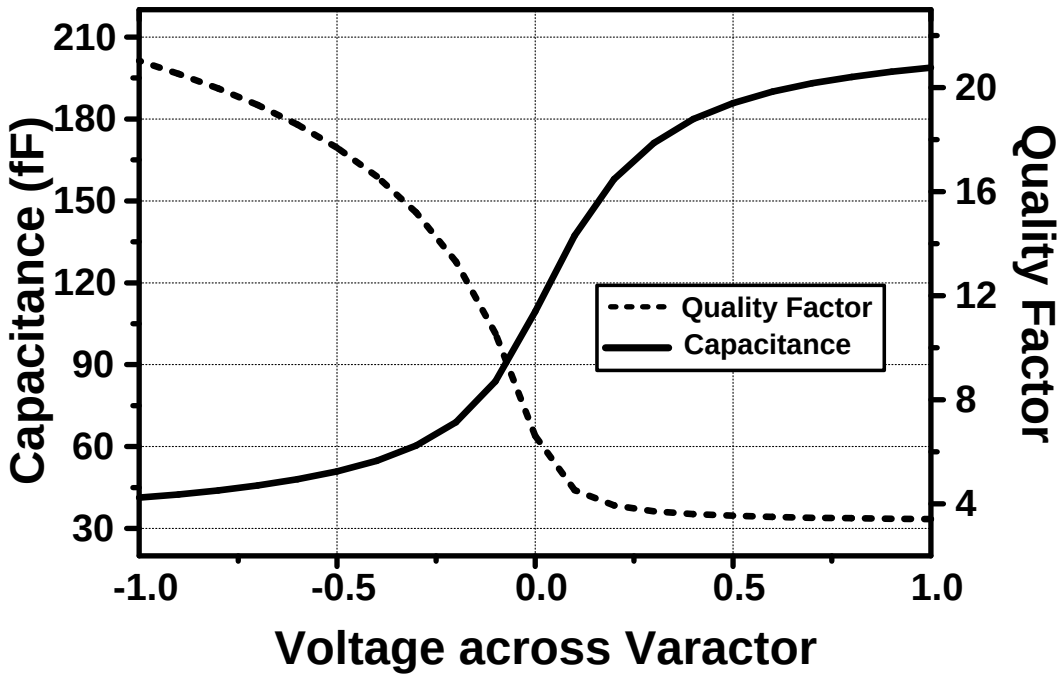

Figure 1.15: Capacitance and quality factor of varactor against various bias voltages.

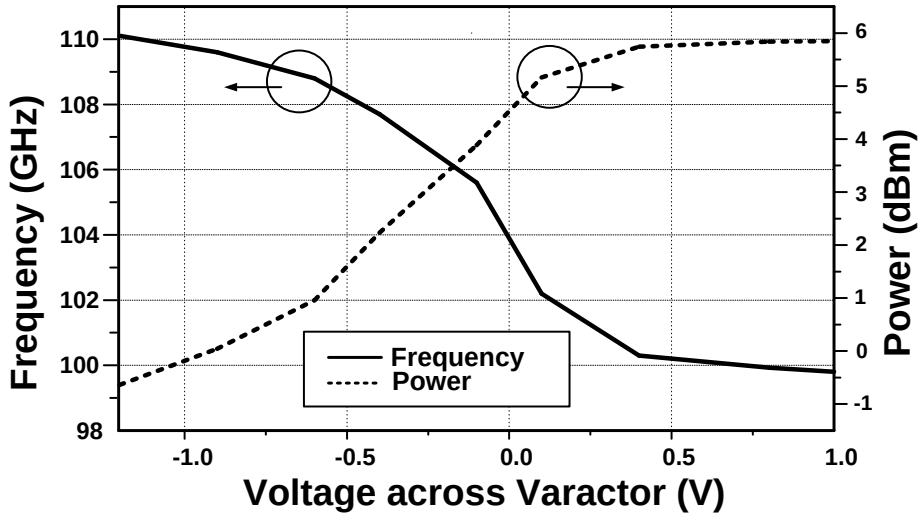

Figure 1.16: Simulated tuning range and output power of designed VCO.

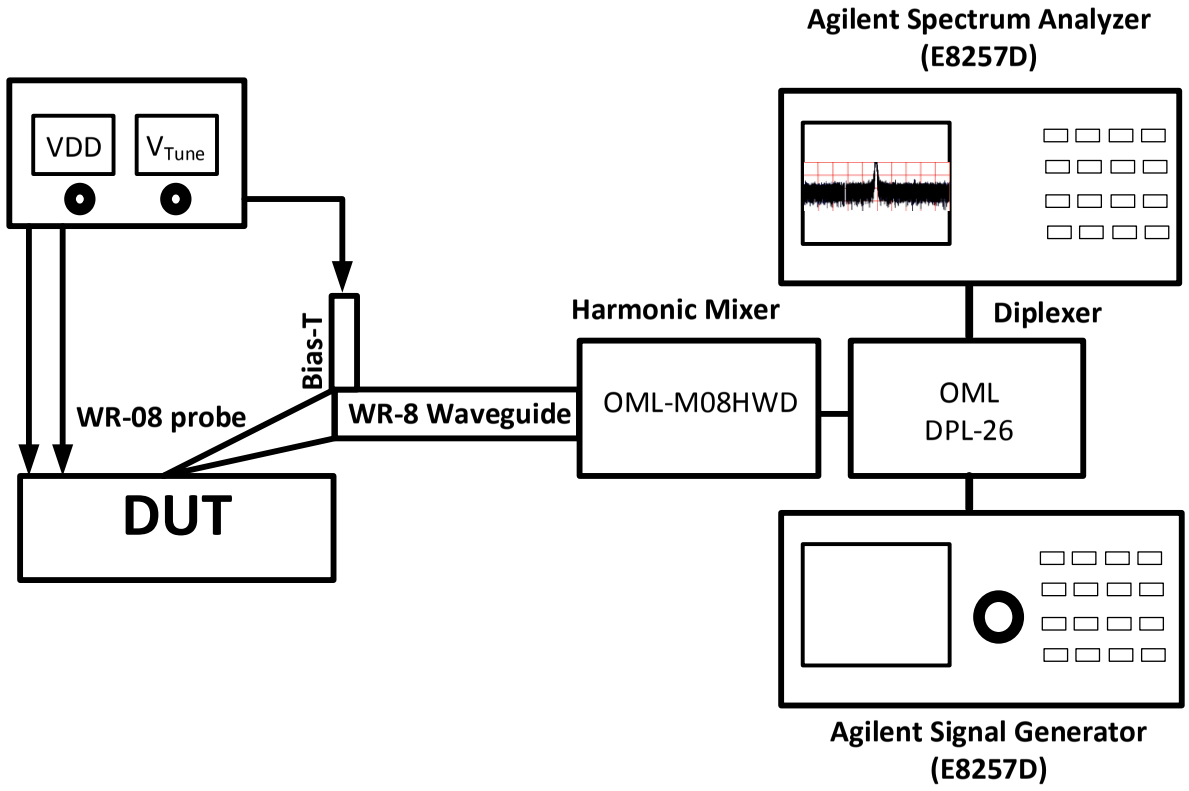

Figure 1.17: Measurement setup.

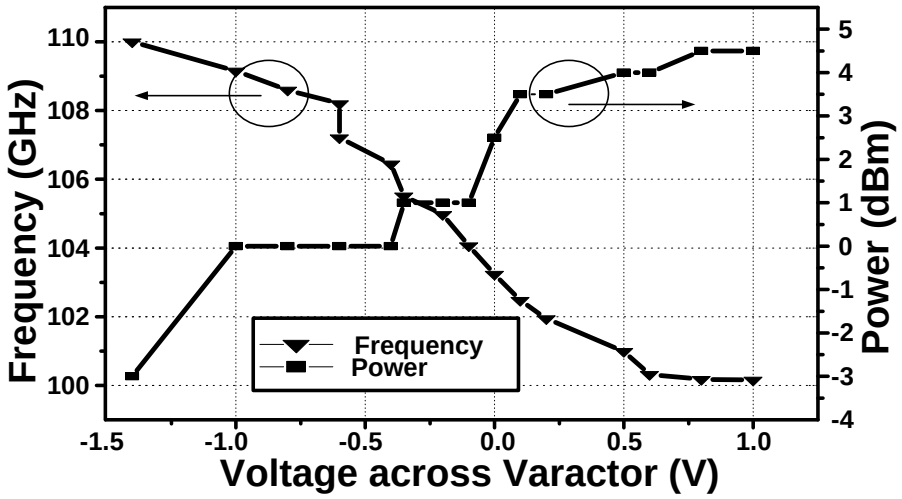

Figure 1.18: Measured Tuning range and output power against various bias voltages.

The oscillator draws 45mA of current from a 1.2V supply. Fig. 1.18 shows the measured output frequency and calibrated output power. The output frequency can be continously tuned from 100GHz to 110GHz. Measured power and tuning range is very close to the simulated results. The maximum measured power is 4.5dBm at 100GHz which is 1.4dB less than our simulations. The output power remains above 0dBm from 100GHz to 109GHz.

Fig. 1.19 and Fig. 1.20 presents the typical spectrum of output at 105GHz and chip photograph. Fig. 1.21 shows measured phase noise at 105GHz. The measured phase noise is -92.83dBc/Hz at 1 MHz offset. Table 1.1 shows the comparison with prior art. This work demonstrates the highest tuning range and output power among the VCOs in the same frequency range implemented in a standard CMOS process.

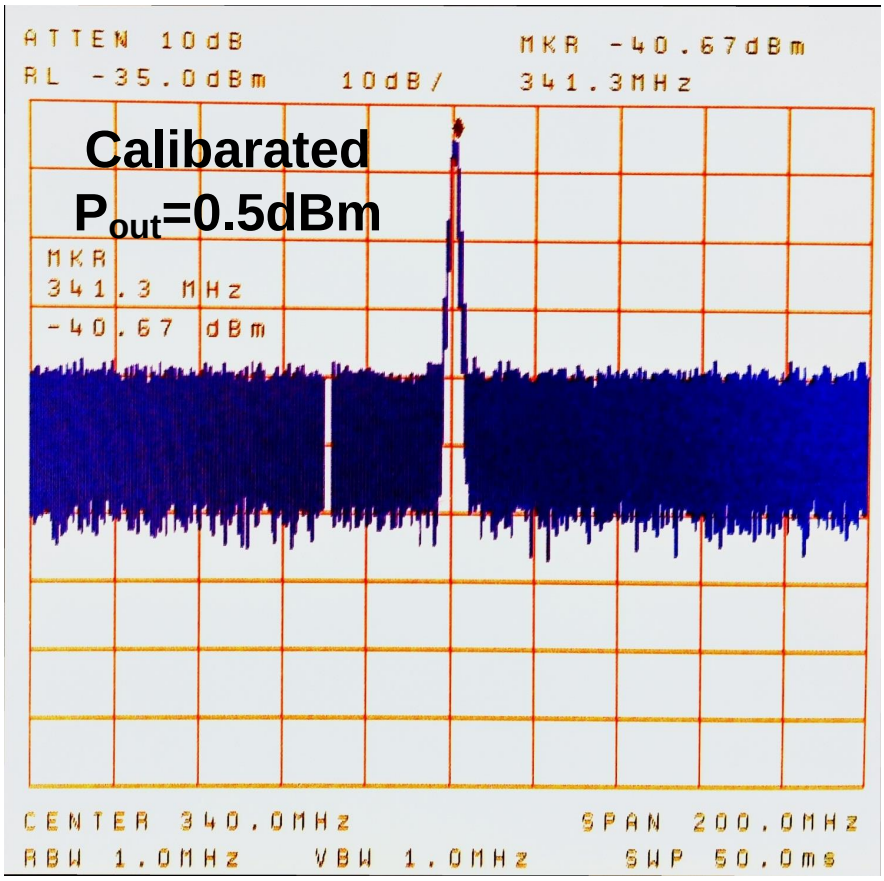

Figure 1.19: Typical measured output spectrum.

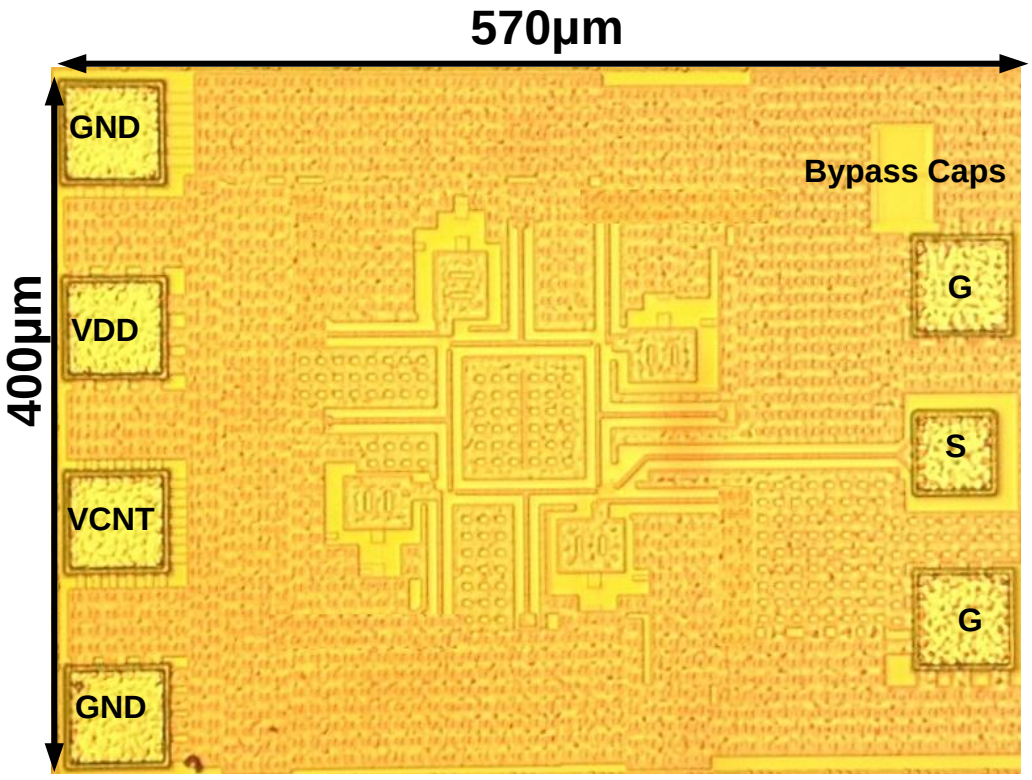

Figure 1.20: Chip photograph

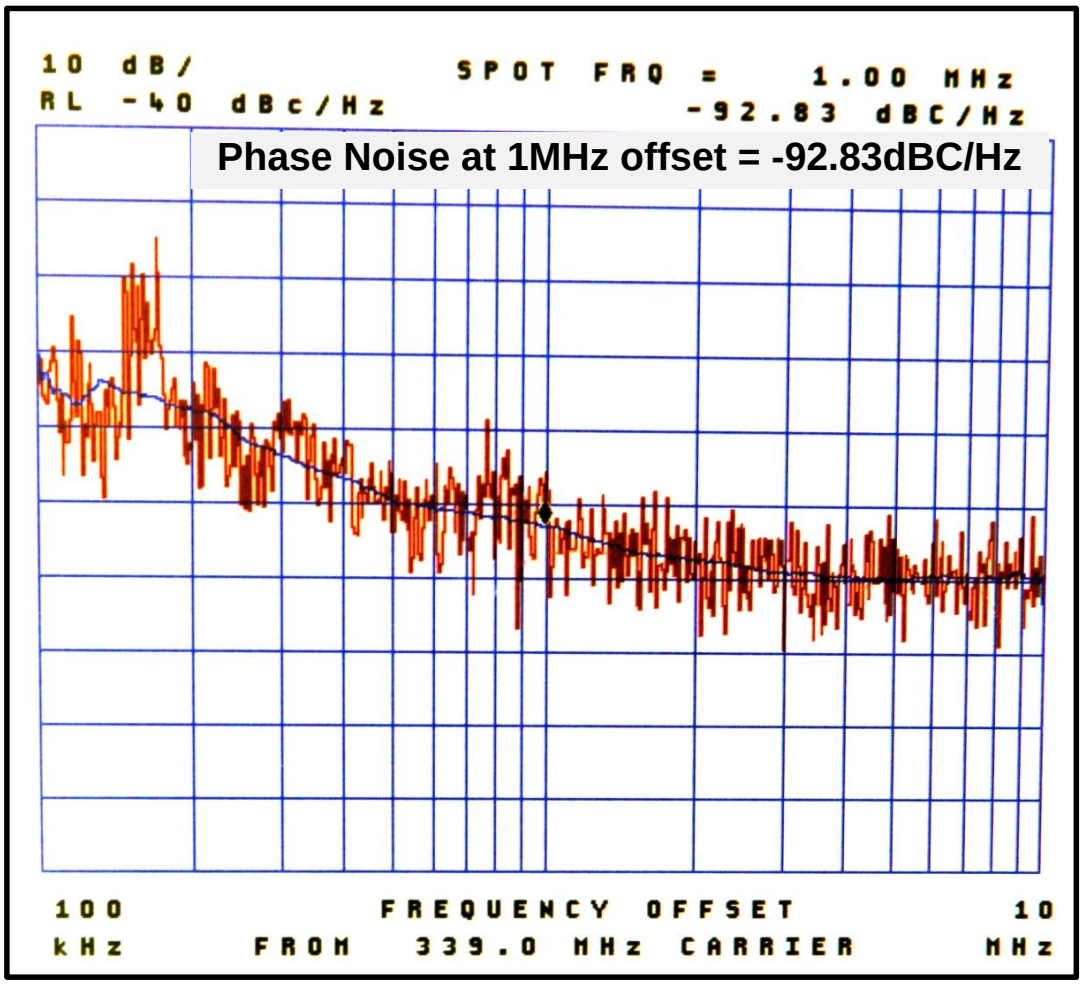

Figure 1.21: Measured phase noise.

Table 1.1: Comparison with Prior Art

Ref	Tech.	Freq (GHz)	Tuning Range	Core P_{DC}(mW)	P_{out} (dBm)	DC-RF %	Phase Noise (dBc/Hz)	FOM_T
[20]	90nm CMOS	104	NA	5.8	-8.2	2.6	Not reported	NA
[21]	65nm CMOS	100.6	4.3%	7.2	-25	0.04	-84.1 at 1MHz	-168.25
[22]	32nm SOI	102.2	4.12%	7.6	-30.65	0.013	-100.8 at 10MHz	-164.48
[18]	130nm CMOS	104	NA	21	-2.7	1.97	-93.3 at 1MHz	NA
[18]	130nm CMOS	121	NA	28	-3.5	2.23	-88 at 1MHz	NA
[23]	65nm CMOS	118.3	7.8%	5.6	-14	0.71	-83.9 at 1MHz	-175.72
This work	65nm CMOS	105	9.5%	54	4.5	5.3	-92.83 at 1MHz	-175.48

1.5 Conclusion

In this work, a loop of unidirectionally coupled oscillators to demonstrate high tuning range and output power is proposed. To achieve large tuning range, two different tuning mechanisms are simultaneously exploited. First each core oscillator is tuned using a variable capacitor. Next, by controlling the phase/delay between the coupled oscillators, the entire loop dynamics and hence its frequency is tuned. In this paper, we analyze a loop of "n" coupled oscillators using Adler's equation and derive the expression for the maximum tuning range. Perturbation analysis is used to study the stability conditions of the loop of coupled system. Activity condition from two port theory is also employed to squeeze maximum power out of active devices. The proposed system is designed and implemented using four coupled Colpitts VCOs in a 65nm bulk CMOS process. The VCO achieves continuous tuning range of 9.5% at the center frequency of 105GHz with the peak output power of 2.8mW. The circuit consumes 54mW from a 1.2V supply. To the best of our knowledge, this VCO has the highest output power and tuning range among all the CMOS oscillators at or above 100GHz.

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CHAPTER 2

A THZ PASSIVELY COUPLED HARMONIC VCO TOPOLOGY WITH HIGH TUNING RANGE AND HIGH OUTPUT POWER

2.1 Introduction

Applications at frequencies ranging from sub-millimeter wave to THz (100GHz to 1THz) are gaining a lot of attention [1] [2]. The applications are not just limited to communication systems as is the case with traditional RF. These high frequencies can be employed for sub-millimeter wave astronomy in the field of heterodyne spectroscopy [3] [4], sensing and imaging for security [5] , detection [6] [7] [8] and communication [9] [10]. Because of the lower f_{max}, scaling of low frequency electronics to high frequencies is very challenging. At the same time, it is very difficult to make efficient semiconductor lasers of wavelength lower than 30μm [11]. Because of the lack of high power and tunable sources at these frequencies, this part of spectrum is usually called "THz gap".

A lot of effort has been done to bridge the "THz gap" both from the electronic side and optics side. Implementation of high frequency sources in CMOS is particularly interesting because of the lower cost of fabrication, high yield and ease of integration with low frequency blocks of the system. Despite fast scaling, f_{max} of transistors in CMOS is still less than 300GHz that gets even lower in the presence of parasitics from interconnects. To overcome lower f_{max}, harmonic generation via device nonlinearity is usually employed. Either frequency multipliers are used or higher order harmonics are collected from a fundamental VCO.

Both frequency multipliers and harmonic oscillators have been exploited in the lit-

erature. A 180GHz active doubler with 3-dB bandwidth of 11.1% is reported in [12]. A 220-275GHz frequency doubler based on a traveling wave topology is proposed in [13], [14] with maximum output power of -6.6dBm. A 480GHz passive frequency doubler using a pair of varactor with the conversion loss of 14.3dB is reported in [15]. In the domain of harmonic oscillator, [16] proposed a non-tunable triple push structure at 256GHz and 482GHz with the output power of -17dBm and -7.9dBm. Also [17]-[18] proposed a VCO based on delayed coupled oscillator at 290GHz with maximum power of -0.5dBm and tuning range of 4.4%. Recently, [19] and [20] proposed a 16-element radiating array with maximum power of 0.5dBm and EIRP of 15.7dBm at 260GHz suitable for spectroscopy.

Though multipliers at high frequencies can be broadband however they need a very high power and tunable source at fundamental frequency which itself is a challenge. For example, the fundamental power required by [14] is 4dBm that produces output of -6.6dBm at 240GHz. Similary, [15] needs a 8dBm fundamental source at 240GHz to produce -6.3dBm at 480GHz. Generating this much fundamental power at tunable fundamental frequencies is very challenging. On the other hand, harmonic oscillators combine the fundamental and harmonic generation functionality in to one structure that simplifies the design. Though oscillators proposed in [16]-[18] were able to produce decent output power levels, however their tunability is very limited.

Simultaneous design of both high tunability and high power is challenging. The low frequency oscillator design methodologies cannot be applied directly at the mm-wave frequencies because in formers case, performance is limited by the quality factor of inductor however in later, varactor limits the performance in terms of output power, tunability as well as phase noise. The output power is strongly affected by the low quality factor of varactor employed in the LC tank for tuning purpose. The typical

value of quality factor of varactor is less than 8 at 120GHz in a 65nm CMOS process. The tuning capability of varactor is severely effected because at high frequencies device parasitics become comparable with the size of varactor. Also in most cases, varactor comes in parallel with the device parasitic capacitances, hence it lowers the maximum oscillation frequency. The existing techniques of magnetic tuning [21] and resonant mode switching [22] cannot be applied at mm-wave frequencies as these schemes rely on switches either inside the tank or in the G_m network which adds extra loss and additional parasitics in "ON" state and in "OFF" state, respectively.

In this work, we combine two mechanisms simultaneously: tuning via variable capacitance and tuning via variable delay of coupled oscillator [23]. To accomplish both, a loop of unidirectional coupled oscillator is employed. Besides providing an extra dimension of tuning, coupling also enhances output power as well as the phase noise. Circuit level implementation of the proposed methodology is realized through a modified self-feeding Colpitts oscillator. The proposed circuit is implemented without any explicit phase shifters. To enhance the fundamental power, two port theory is used to study the activity condition of active devices. The results of the activity condition are used to maximize the power produced by transistors. The fundamental frequency is chosen to be around 130GHz and second harmonic is extracted. To maximize the second harmonic power at the output all the unnecessary leakage of second harmonic current is blocked. We build two prototypes consisting of a loop of two and eight oscillators. The 2-stage and 8-stage VCO achives maximum power of -2.5dBm and 3.5dBm with DC-RF efficiency of 0.9% and 0.8%. Both VCO achieve tuning range of 8.6% at 260GHz. To the best of our knowledge, these VCOs have the highest output power, tuning range and DC-RF efficiency among all the CMOS oscillators at or above 0.25THz.

The rest of the paper is organized as follows: Section II describes the architecture

of a system of coupled oscillators to achieve maximum tunability and power. Section III introduces the modified self-feeding architecture that meets all the requirements presented in section II. Section IV and section V presents the design and simulation of two stage and eight stage coupled system respectively. Conclusion and comparison with prior art is presented in section VI.

2.2 Architecture of coupled harmonic oscillators

In this work, we employ a system of coupled oscillators as shown in Fig. 2.1. The core consists of a unidirectional loop of coupled oscillator with variable coupling blocks. The harmonics are generated at each oscillator via nonlinearity of the transistors and they are extracted at the output. An efficient THz source must satisfy few requirements. 1) The core should have desired tunability at the fundamental frequency. 2) The core should be able to generate maximum fundamental power as higher fundamental power corresponds to greater harmonic currents. 3) The core architecture should avoid all the unnecessary leakage of desired harmonic current. 4) The output matching network should block all the undesired harmonics and provide appropriate matching for the desired harmonic. The following subsections describe the methodologies we employed to meet these aforementioned requirements.

2.2.1 Enhancing the tuning range

Adler presented dynamics of a system of coupled electrical oscillators in the context of injection locking [24]. When a free running oscillator at ω_o is injected with a signal from another oscillator at ω, under certain conditions the first oscillator locks to second

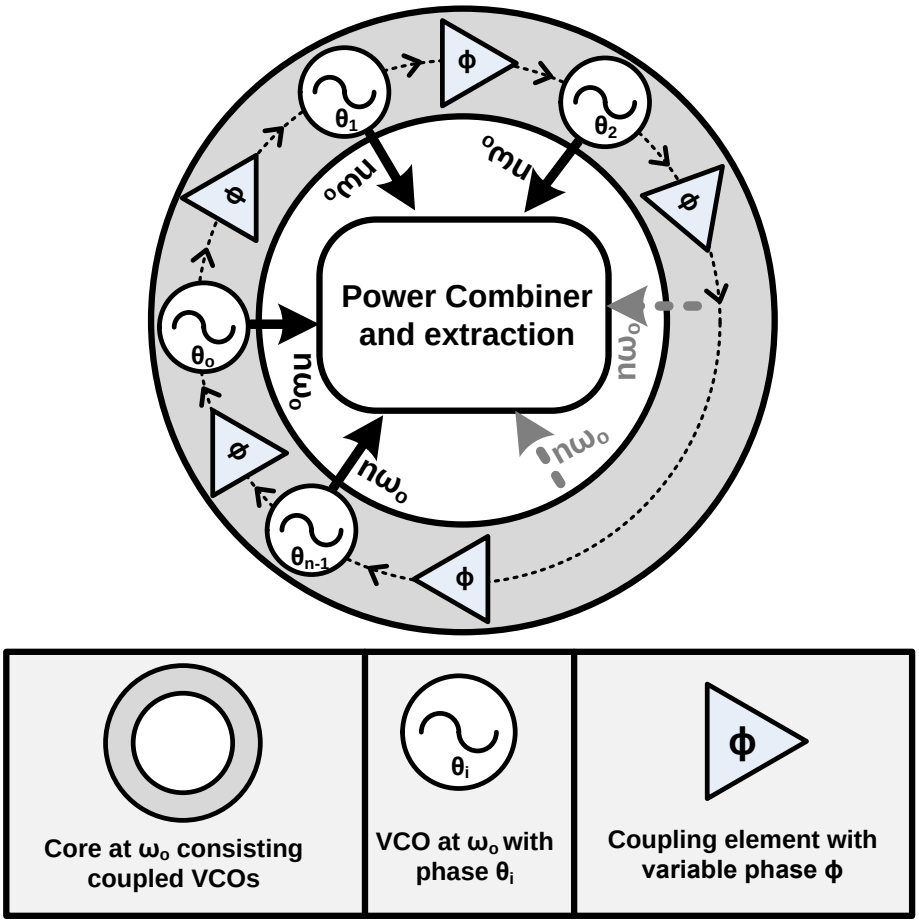

Figure 2.1: A loop of coupled oscillator with n_{th} harmonic extraction.

oscillator at ω. This locking results in a phase difference ($\Delta\phi$) between two oscillators which is proportional to the frequency difference ($\Delta\omega = \omega - \omega_o$) given by

$$\Delta\phi \quad = \quad sin^{-1}\left(2Q\frac{I_{core}}{I_{inj}}\frac{\Delta\omega}{\omega_o}\right) \tag{2.1}$$

where Q is the quality factor of the resonator and I_{core} and I_{inj} are the currents inside core and injected from the outside, respectively. Conversely, the oscillation frequency of two mutually coupled oscillators can be controlled by enforcing a certain phase shift between them.

We employ two kinds of tuning mechanism in the system shown in Fig. 2.1. 1) Local tuning: this is implemented at the level of individual oscillators using varactors inside each core. When the varactor the tuned it changes the local/individual frequency of each oscillator. 2) Global tuning: It is achieved at the system level where frequency variation is performed by changing the coupling between core oscillators. In Fig. 2.1, coupling phase, ϕ is varied to achieve global tuning. In this work, we design the system in such a way that the overall tuning range is the addition of both approaches.

The oscillation frequency of any system similar to Fig. 2.1 is found to be [25] [26]

$$\omega \quad = \quad \omega_o\left(1 + \frac{\Delta C}{2C_o}\right) + K_s sin(\phi - (\theta_i - \theta_{i-1})) \tag{2.2}$$

where $K = \frac{I_{inj}}{I_{core}}\frac{\omega_o}{2Q}$ is the coupling factor and ϕ is the phase shift resulting from the phase shifter in Fig. 2.1. The maximum tuning range can occur when the argument of sine in (2.2) changes from $-\pi/2$ to $\pi/2$, hence

$$\left.\frac{\Delta\omega_{max}}{\omega_o}\right|_{local+global} \quad = \quad \frac{\Delta C_{max}}{C_o} + \frac{I_{inj}}{I_{core}}\frac{1}{Q}, \tag{2.3}$$

which comes out to be sum of capacitive as well delayed coupled oscillator tuning.

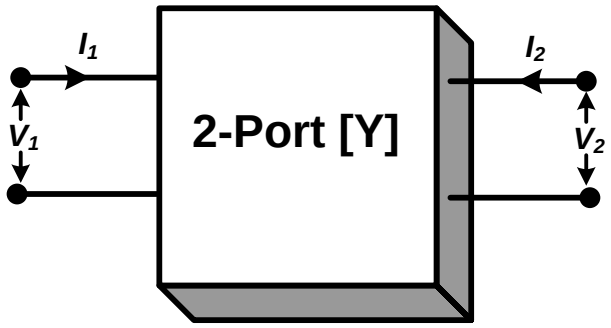

Figure 2.2: Two port Y-parameter model to derive activity condition.

2.2.2 Obtaining maximum power - Activity condition

To achieve maximum power coming out of the active devices in VCO design, we look at the activity condition from the perspective of two port theory [27][16] Now the power coming out of two port network shown in Fig. 2.2 can be written as

$$P_{out} = -Re(V_1 I_1^*) - Re(V_2 I_2^*)$$

We can plug in the values of I_1 and I_2 from the Y matrix.

$$\begin{aligned} I_1 &= Y_{11}V_1 + Y_{12}V_2 \\ I_2 &= Y_{21}V_1 + Y_{22}V_2. \end{aligned}$$

Assume,

$$A = \frac{V_2}{V_1}$$

and g_{ij} and b_{ij} as the real and imaginary part of Y_{ij} then:

$$P_{out} = -g_{11}|V_1|^2 - g_{22}|V_2|^2 - |V_1||V_2|\left((g_{12} + g_{21})cos\angle A - (b_{21} - b_{12})sin\angle A\right).$$

In case of oscillators, magnitude of voltage gain A is usually unity, however phase is extremely important and is given by

$$\angle A_{opt} = \angle - (Y_{21} + Y_{12}^{*}) . \tag{2.4}$$

2.3 Circuit level realization of proposed system

The implementation of both global and local tuning in one system is challenging. We modified the self-feeding Colpitts topology presented in [19][20] to implement each oscillator of Fig. 2.1 because, as explained later, it allows us to implement global tuning without any explicit phase shifters hence resulting in a simpler implementation. The standard and modified self-feeding Colpitts is shown in Fig. 2.3. In the self-feeding oscillator the signal at the drain is fed to gate via a transmission line of phase ϕ and impedance Z_o. The length of transmission line majorly defines the oscillation frequency of this oscillator too. It is noteworthy that the transmission line between the gate and the drain carries both travelling wave and standing wave. The modified self-feeding Colpitts has a varactor at the source of the transistor which performs local tuning. Moreover the varactor comes in series with the parasitic capacitance between gate and source, C_{gs}, hence it does not decrease the oscillation frequency of the oscillator.

2.3.1 Global Tuning

We passivey couple "n" harmonic oscillators as shown in Fig. 2.4. The transmission line with phase ϕ_c and impedance Z_c are used to couple multiple oscillators. The desired harmonic is extracted via a transmission line of ϕ_d and impedance Z_d.

The energy from each oscillator is injected from the gate of transistor in to the next

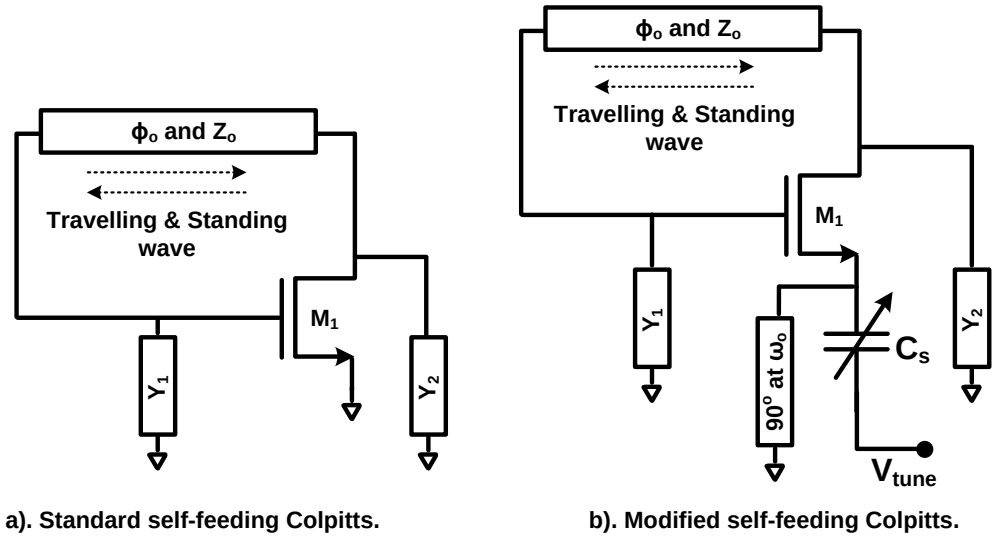

Figure 2.3: Standard and modified self-feeding Colpitts

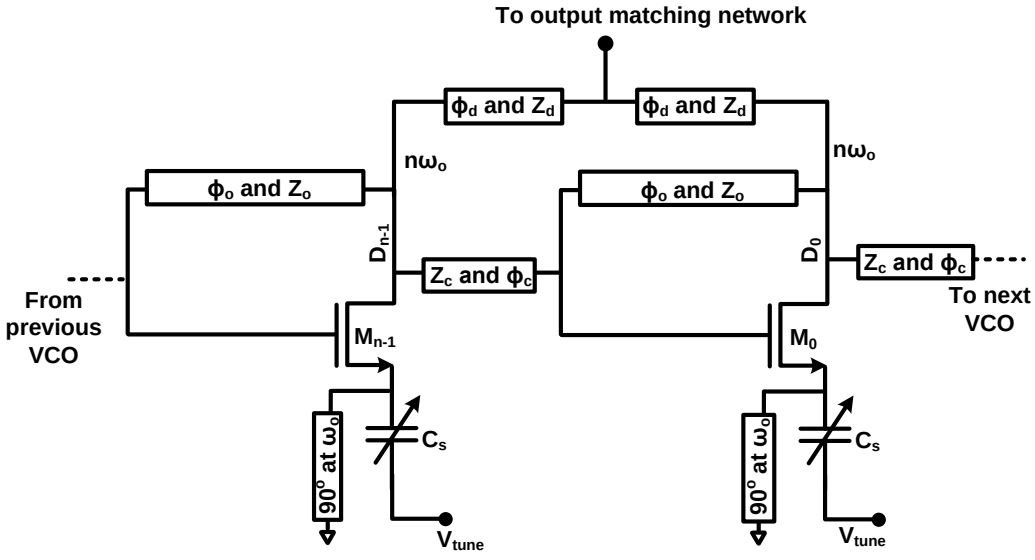

Figure 2.4: Couping multiple self feeding harmonic oscillators.

stage via the drain current. The varactor inside each core also varies the phase of injected current along with changing the oscillation frequency of the system. The change in phase performs global tuning.

We look at the phase of Y_{21} of a transistor with capacitor at the source in order to understand global tuning in Fig. 2.5. A 20μm wide transistor in a 65nm CMOS process is simulated with capacitor at the source. The phase of Y_{21} is plotted at 120GHz in Fig. 2.5 against capacitance at the source. Recall from the last section that phase delay corresponds to global tuning:

$$\left.\frac{\Delta\omega_{max}}{\omega_o}\right|_{global} = K sin(\theta_{delay}). \tag{2.5}$$

From Fig. 2.5, two effects happen with change in capacitance. Consider the case of decrease in capacitance: i) it increases the local frequency of each oscillator of Fig. 2.4. ii) it increase the phase or decreases the delay of Y_{21} from (2.5), that results in increases of frequency of the coupled system even more. Both effects add constructively in our design.

2.3.2 Optimum phase condition

The self-feeding oscillator presented in Fig. 2.3 can achieve optimum phase condition. Consider Y represents the two port Y-parameter of a transistor with g_{ij} and b_{ij} representing the real and imaginary part of Y_{ij} and A_I and A_R represent the imaginary and real part of optimum phase derived through (2.4) then the self-feeding oscillator can meet optimum phase condition with appropriate ϕ_o and Z_o in Fig. 2.3 such that

$$Z_o sin(\phi_o) = \frac{Re(A_I)}{g_{11} + Re(A.y12)}. \tag{2.6}$$

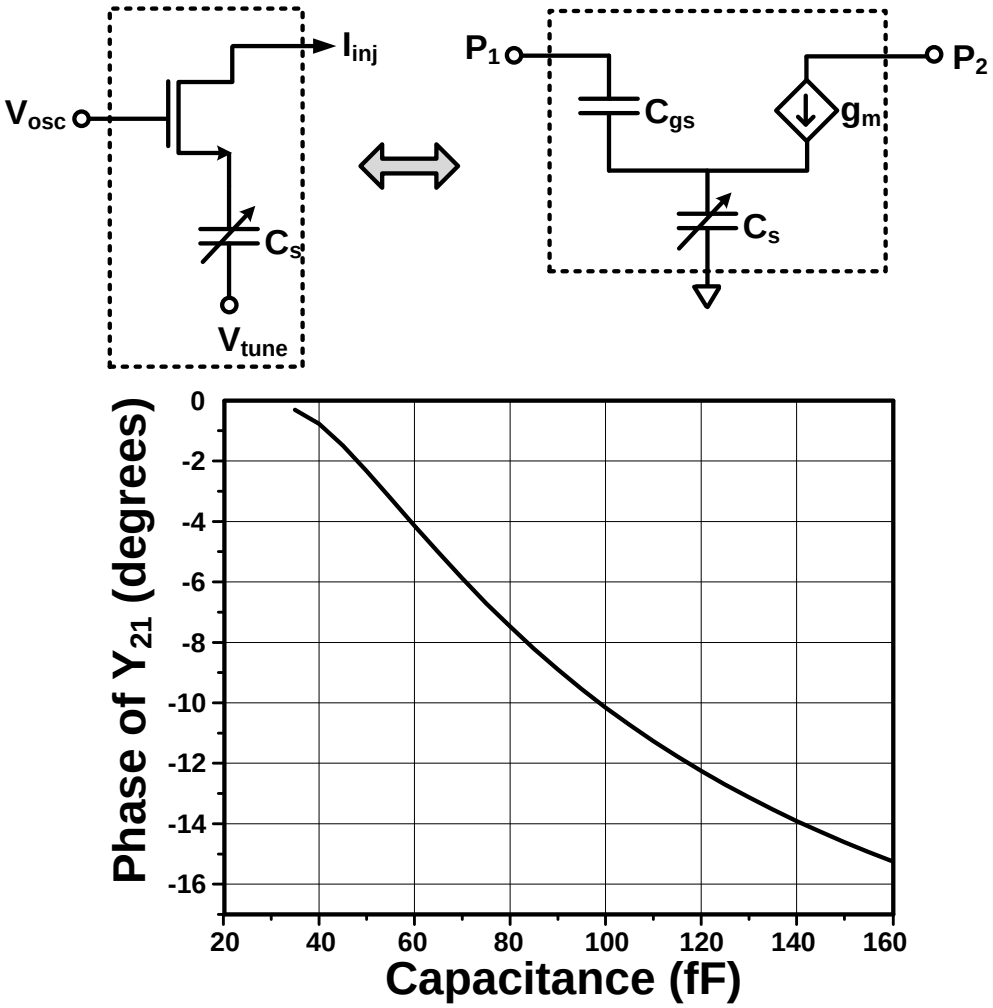

Figure 2.5: Simulated phase of Y_{21} against capacitance at 120GHz

However, in the modified self-feeding Colpitts transistor is no more a two port device as it has a capacitor at the source. In order to apply results presented in (2.4) and (2.6) we must convert the transistor with capacitor at the source (Fig. 2.6) in to a two port network. We can break such a series network in to two two-port networks as shown in Fig. 2.6.

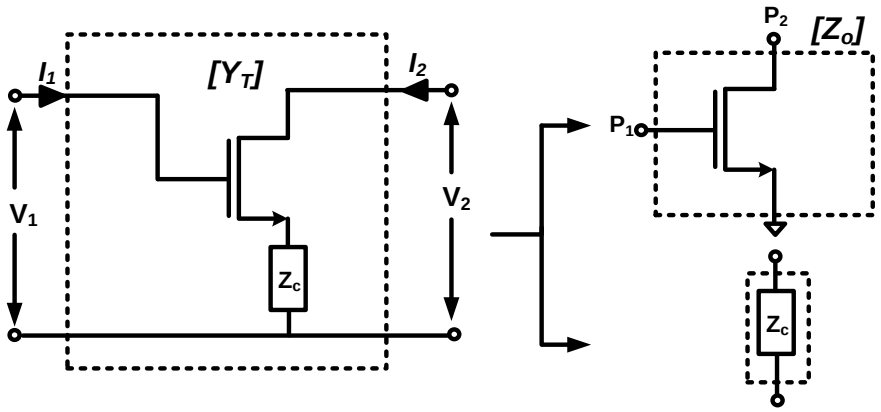

Figure 2.6: Two port network of a transistor with the capacitor at the source.

$$\begin{aligned} \left[Z_T\right] &= \begin{bmatrix} Z_{T11} & Z_{T12} \\ Z_{T21} & Z_{T22} \end{bmatrix} \\ \left[Z_T\right] &= \left[Z_o\right] + \begin{bmatrix} Z_c & Z_c \\ Z_c & Z_c \end{bmatrix}. \end{aligned} \tag{2.7}$$

Y-parameters of the network under study can be found using

$$\left[Y_T\right] = \left[Z_T\right]^{-1}.$$

Hence we can replace the Y parameters involved in (2.4) and (2.6) with Y_T and apply the results for modified self-feeding Colpitts.

2.3.3 Efficient harmonic extraction

Fig. 2.4 shows the harmonic extraction principle. We extract second harmonic using transmission line of impedance Z_d and phase close to 90^o. Such configuration enforces out of phase operation of adjacent oscillators because only in out of phase operation, 90^o

lines transform virtual ground at the common mode to open at the drain of the transistors. On the other hand, for in-phase operation oscillators see relatively smaller impedance at the drain hence in-phase operation is not supported.

For efficient operation, it is important to extract all the harmonic current at the output. For instance, consider a typical ring oscillator as shown in Fig. 2.7(a). The second harmonic current generated at the drain is divided between the output and the gate of next stage. At frequencies close to f_{max}, C_{gs} presents lower impedance (Z_g) as shown in the smith chart. Hence a part of second harmonic current is wasted. The situation becomes even worse with the small interconnect present between the drain and gate and Z_{leak} seen at the drain is even lower than the Z_g.

The modified self-feeding Colpitts enhances harmonic extraction by blocking the leakage of second harmonic current as shown in Fig. 2.6(b). The transmission line TL_o not only serves as the self feeding path but also transform Z_g of the it own transistor from 14Ω to open. At the same time, the coupling transmission line TL_c transforms the impedance of gate of next oscillator to 61Ω which is about four times higher than present in standard double-push ring oscillator (Fig. 2.7(a)).

2.4 Design of 2-stage and 8-stage prototype

Based on the proposed methodology, we design two prototypes consisting of a loop of two and eight self-feeding VCO. The schematic of 2-stage and 8-stage is shown in Fig. 2.8 and Fig. 2.9. The prototype is designed in a 65nm TSMC CMOS process. The top metal in this process is $3.4\mu m$. All the transmission lines are implemented using top metal as coplanar waveguides with ground shielding except the ones used for output extraction in eight stage oscillator. The ground shielding is implemented by combining

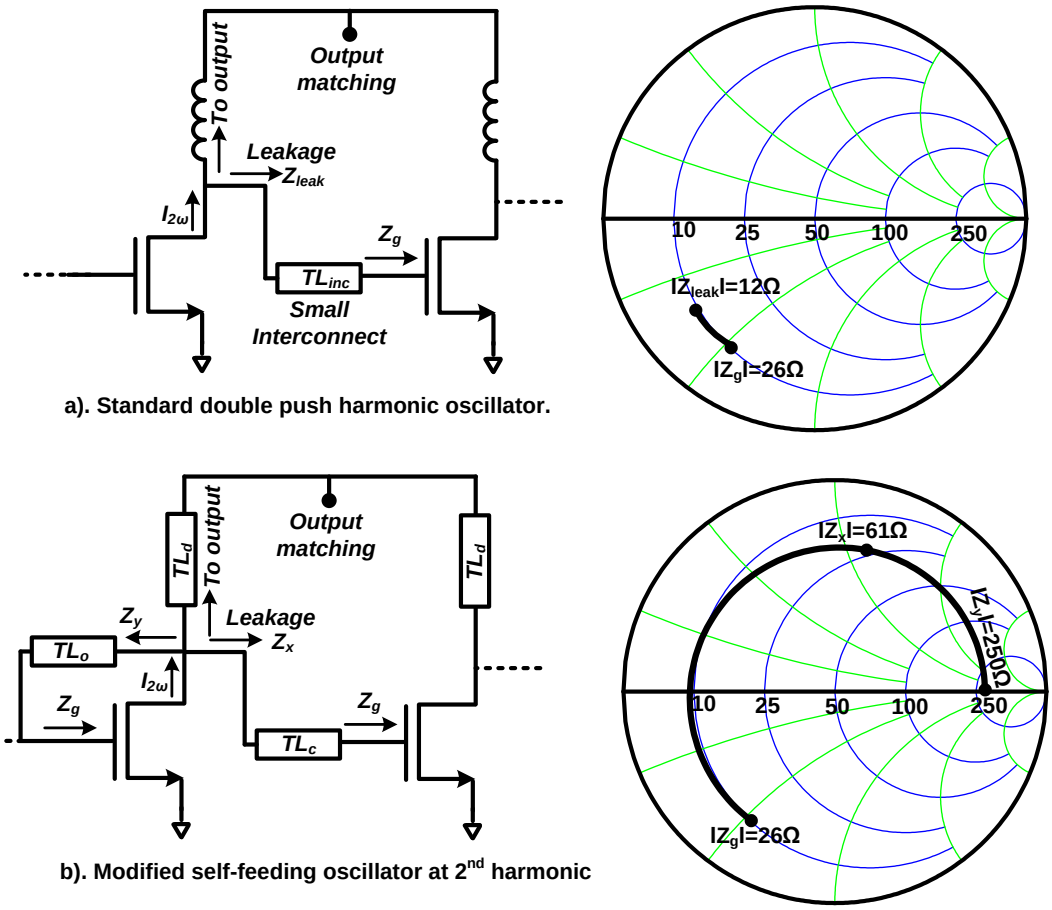

Figure 2.7: 2^{nd} harmonic efficiency in standard ring oscillator Vs. in self-feeding Colpitts

lower two metals for low resistance. All the dimensions of line are shown in Fig. 2.8 and and Fig. 2.9.

In order to see the effect of global tuning in designed prototype, an open loop tuning range and the closed loop tuning range is plotted in Fig. 2.10. As can be seen in Fig. 2.10, the oscillation frequency goes down when we close the loop. This happens because of the inclusion of another boundary condition i.e. the phase shift across the loop must

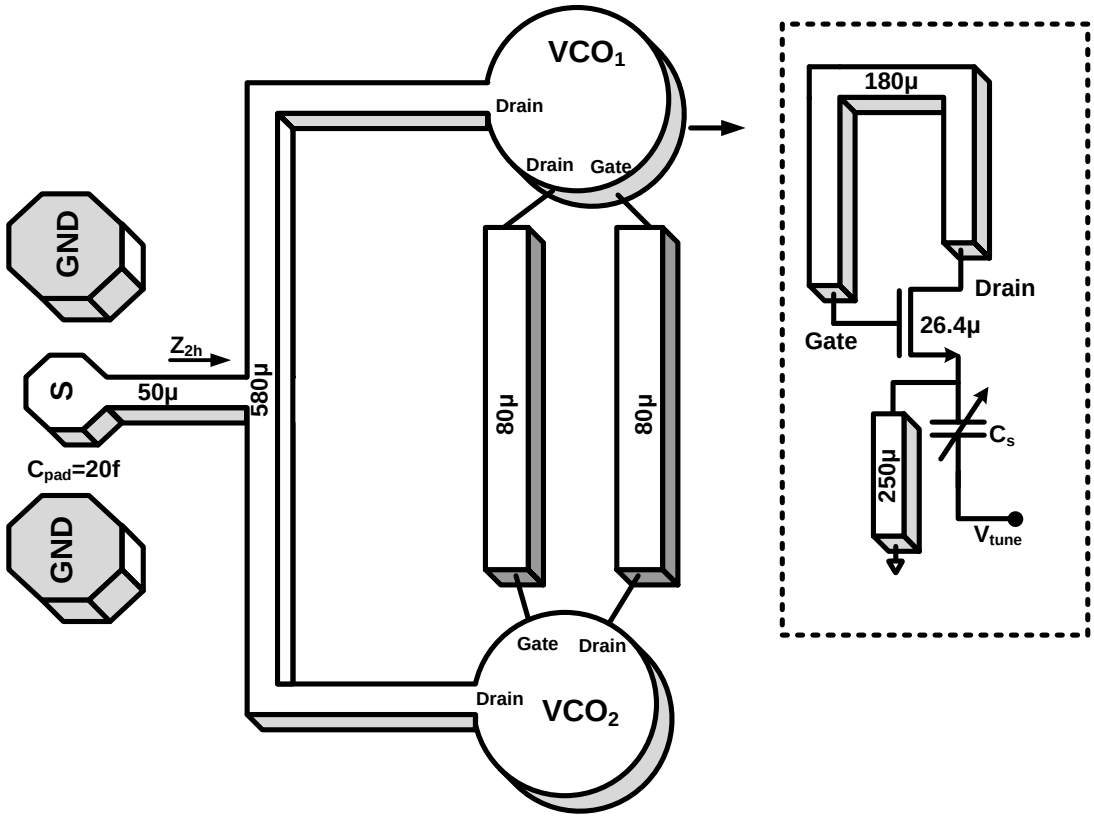

Figure 2.8: Schematic of two stage VCO.

be multiple of 2π. Fig. 2.10 further tells that the global tuning enhances the tuning range by 4%. Even though we are not incorporating explicit phase shifter, the proposed topology enhances tuning range by 1.8 times over pure capacitive tuning.

In order to squeeze maximum power out of transistors, we employ optimum phase matching condition derived in (2.4) using the Y-parameters in (2.8) for 26.4μ wide transistors employed in 2-stage and 8-stage oscillator. The optimum phase came out to be -165^o at the center frequency. Here we are interested in how much achieved phase in our designed prototype varies from the theoretical value calculated via (2.4) over all

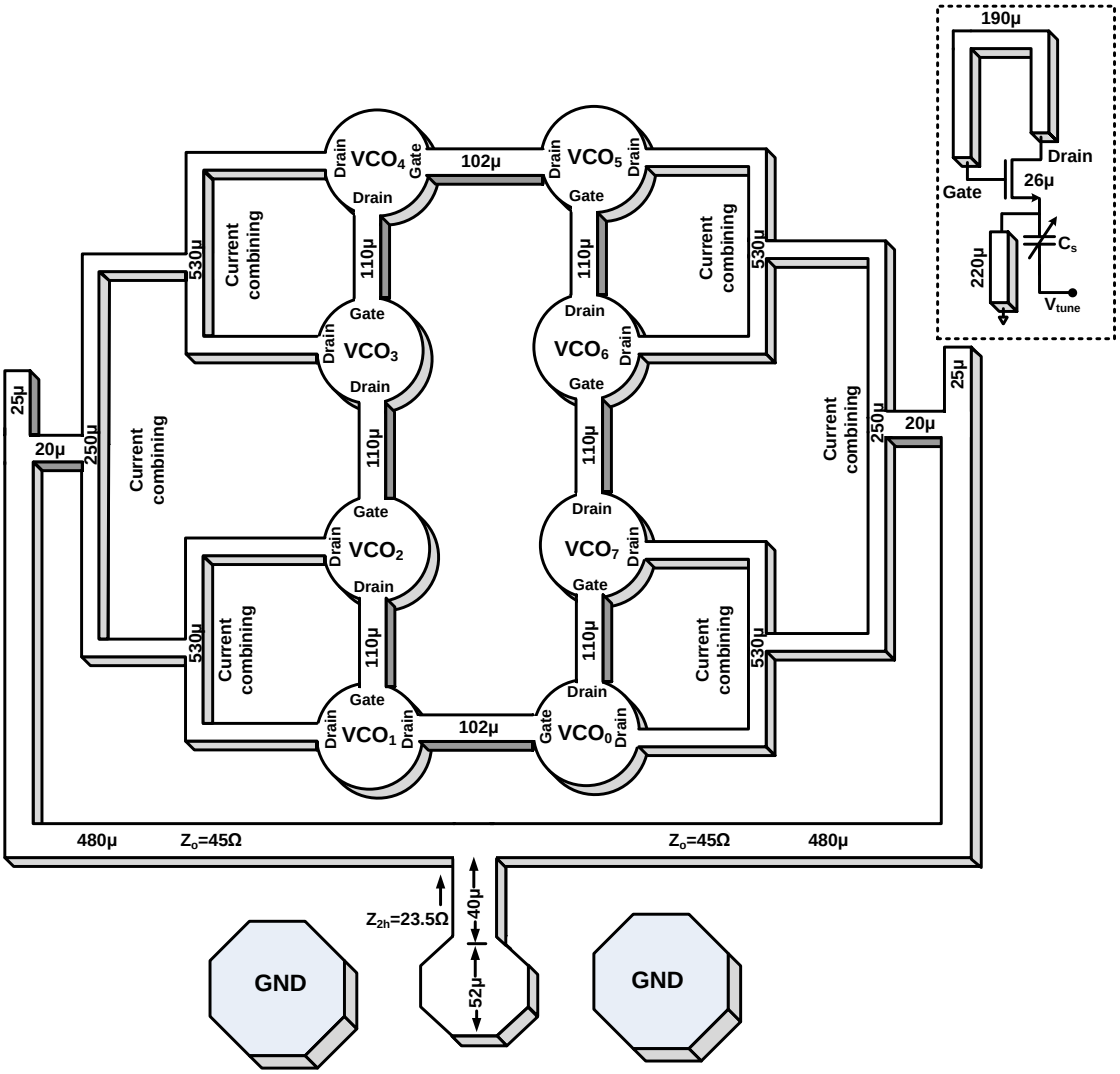

Figure 2.9: Schematic of eight stage VCO.

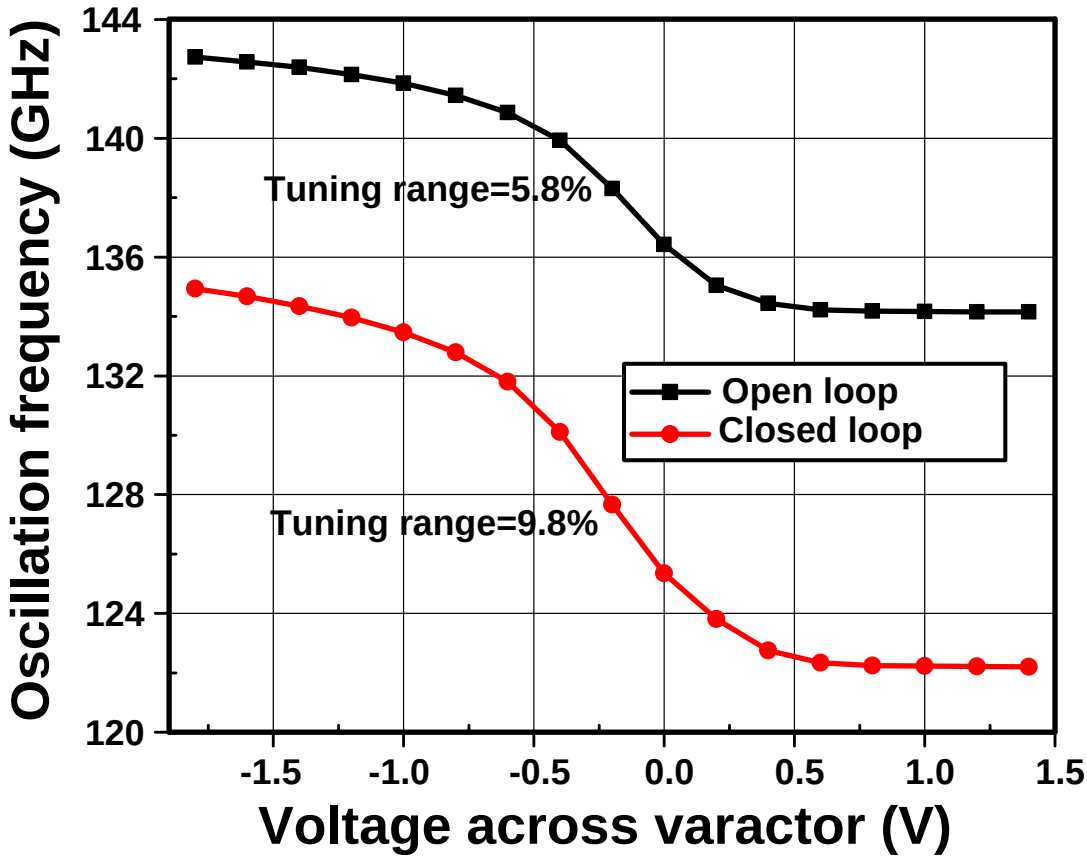

Figure 2.10: Open loop and closed loop tuning range.

the tuning range. Fig. 2.11 plots this variation for the 2-stage and 8-stage VCOs. As shown in Fig. 2.11, the optimum phase variation is between -18^o and 19^o. In order to understand how much this phase variation affects the maximum power coming out of the transistors, we plot maximum power against phase of the employed 2-port device represented by (2.8) in Fig. 2.12. As can be seen in Fig. 2.12, the output power variation is less than $0.2dB$ within our design region. The design of appropriate output matching is challenging. The required pad capacitance is about 18fF however because of smaller distance between the top metal and bottom metal the smallest pad capaci-

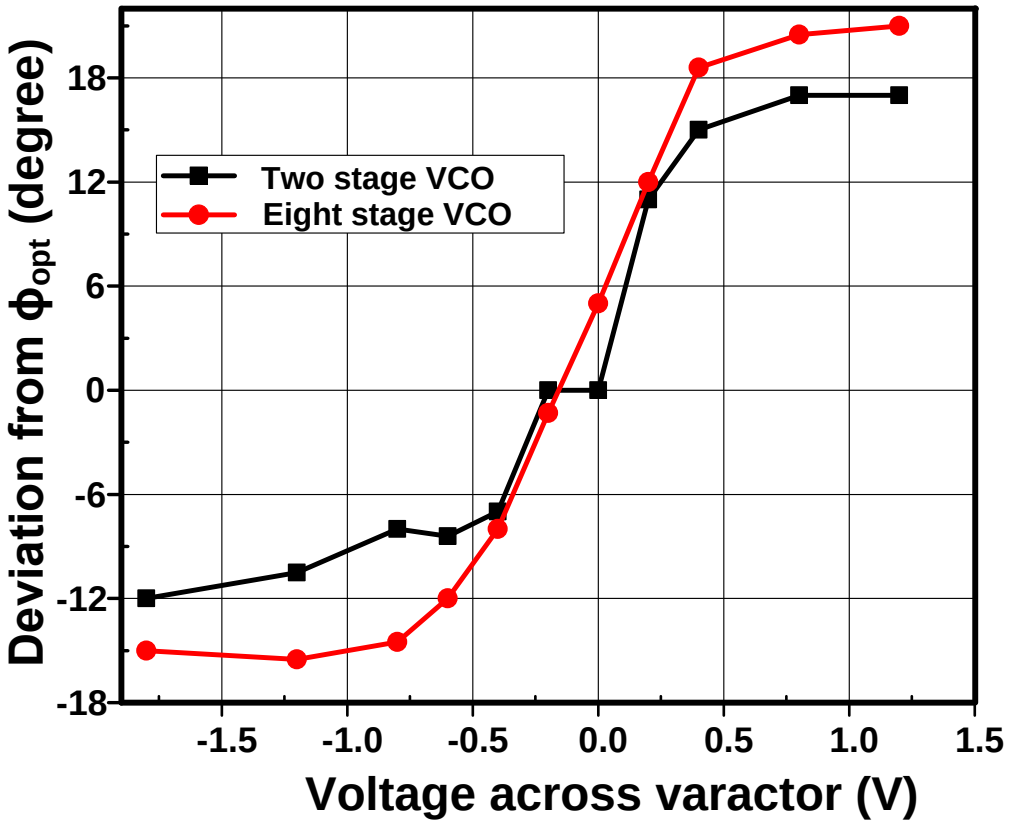

Figure 2.11: Optimum phase Vs. phase achieved in our designed prototypes.

tance we achieve for 40μx40μ is about 24fF. The achieved matching and return loss for second harmonic is shown in Fig. 2.13. Similary for 8-stage, the matching is performed at various levels of power combining. The combining stages from 4-to-2 and 2-to-1 is very important for two reasons. First, as can seen in Fig. 2.9, the transmission lines in 4-to-2 stages are very long, so any standing wave in these lines results in additional loss. Second, these combining stages carry a lot of DC as well as AC current so any resonance behavior in these lines can cause excess heating and even melting of metals.

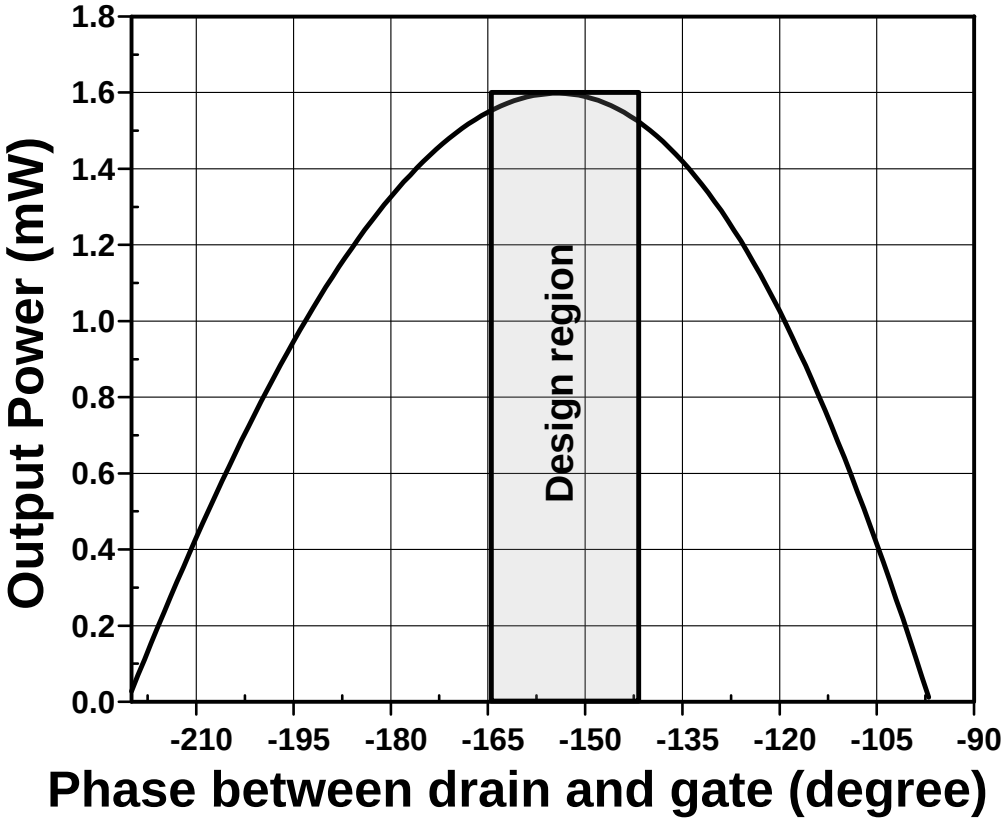

Figure 2.12: Net P_{out} Vs. phase when both drain and gate are excited with a voltage source of 0.8V.

We use open stub for intermediate matching in 4-to-2 power combiner. The 4-2 power combiner consists of 46Ω transmission line. Hence 2-to-1 power combiner is matched from 46Ω to 50Ω. The transmission lines in the last stage is implemented as a $8\mu m$ wide coplanar waveguide that is gradually tapered in to a 40μx40μ pad. The pad is implemented without any ground sheilding to have very low signal-to-substrate capacitance. The last stage matching of 8-stage VCO is shown in Fig. 2.14. The final simulation results for output power and frequency for two-stage and eight-stage VCOs are shown

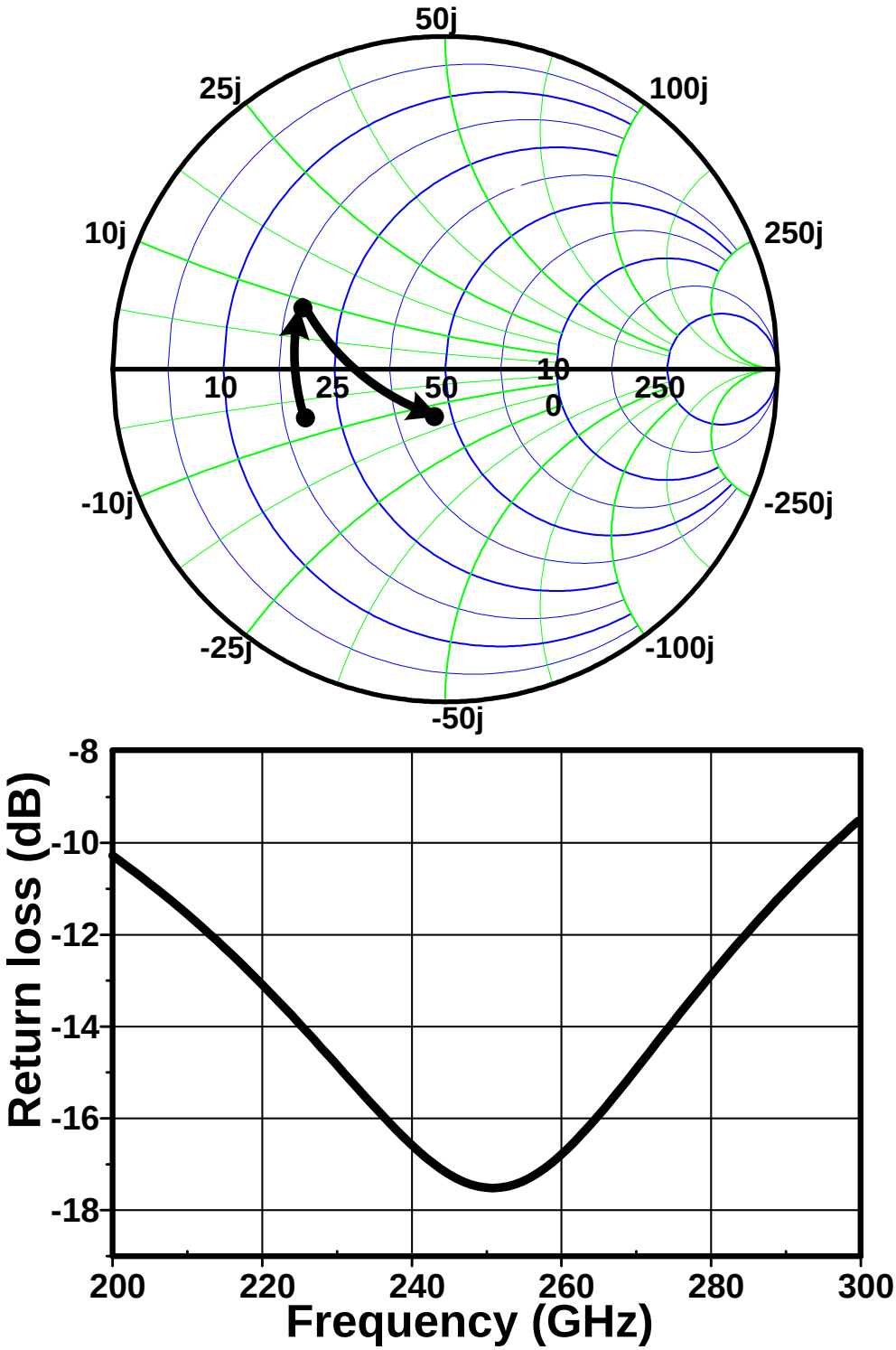

Figure 2.13: Output matching of 2-stage and simulated return loss.

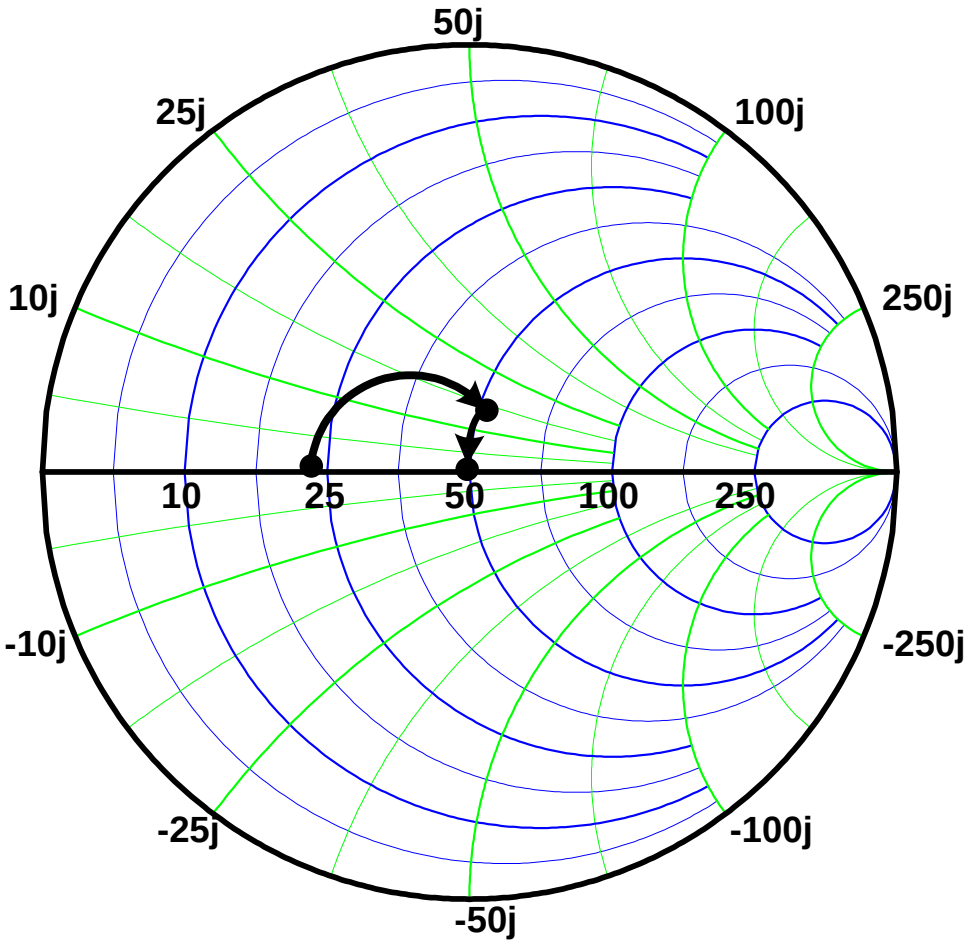

Figure 2.14: Last stage matching of 8-stage VCO.

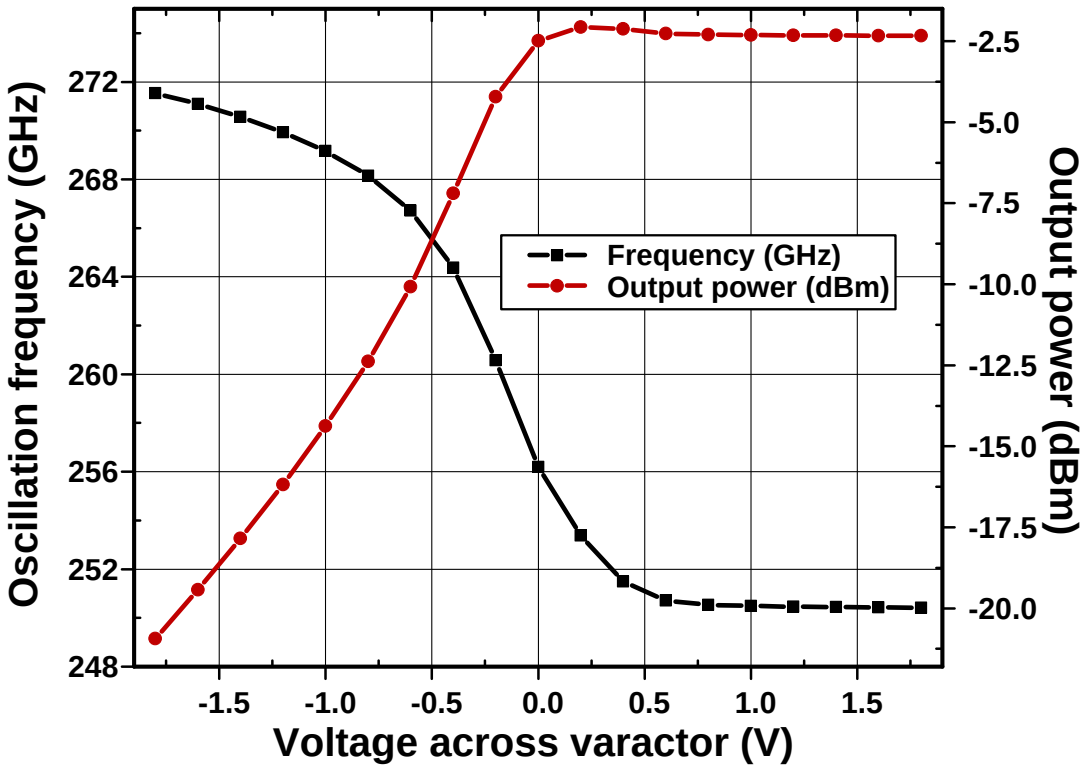

Figure 2.15: Output power and frequency of two-stage VCO.

in Fig. 2.15 and Fig. 2.16 respectively. The output frequency of two-stage VCO can be tuned from 249.5GHz to 272GHz and the maximum power achieved is $-2.12dBm$. Similary, The output frequency of eight-stage VCO can be tuned from 245.5GHz to 268GHz and the maximum power achieved is $3.8dBm$.

The comparison of our work with prior art is shown in table 2.1.

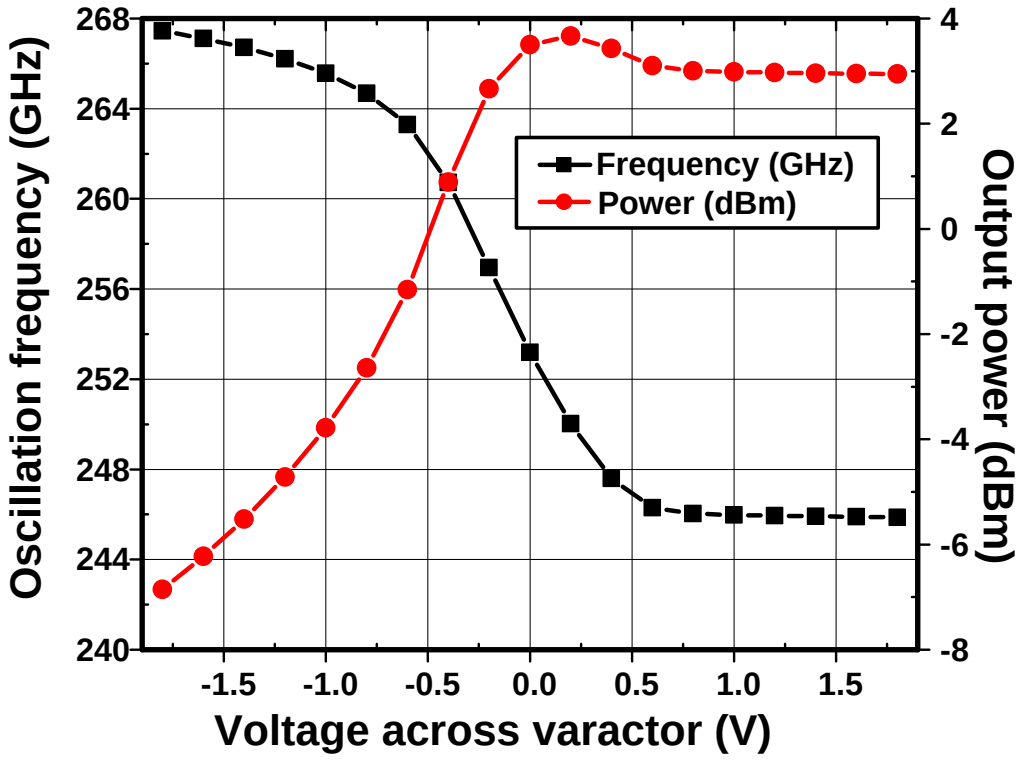

Figure 2.16: Output power and frequency of eight-stage VCO.

2.5 Conclusion

In this work, a loop of unidirectionally coupled harmonic oscillators is proposed to demonstrate high tuning range and output power. To accomplish large tunability, tuning via variable capacitance and via variable coupling delay between oscillators are simultaneously exploited. A large fundamental power to produce high second harmonic is generated using activity condition of the transistors derived through two port theory. All the undesired leakage of second harmonic current is blocked thus extracting maximum power at the output. A passive coupling between VCOs is employed to enhance DC-RF

Table 2.1: Comparison with prior art

Ref	Tech.	Freq (GHz)	TR	P_{DC}(mW)	P_{out} (dBm)	DC-RF %
[18]	65nm CMOS	290	4.5 %	325	-1.2	0.23
[18]	65nm CMOS	320	2.6 %	339	-3.3	0.13
[28]	45nm SOI CMOS	291	NA	19	-13.9	0.21
[29]	130nm SiGe	184.2	2%	95	-11	0.08
This work	65nm CMOS	260	8.6%	58	-2.2	1.03
This work	65nm CMOS	258	8.6%	237	3.7	0.98

efficiency. Each oscillator is realized with modified self-feeding Colpitts architecture. To demonstrate our methodology, a two stage and an eight stage second harmonic VCOs are designed and fabricated in a 65nm bulk CMOS process. The 2-stage and 8-stage VCO achives maximum power of -2.1dBm and 3.7dBm with DC-RF efficiency of 0.9% and 0.8%. Both VCO achieve tuning range of 8.6% at 260GHz. The two stage and eight stage VCO consume 198mA and 49mA from a 1.2V DC supply. To the best of our knowledge, these VCOs have the highest output power, tuning range and DC-RF efficiency among all the CMOS oscillators at or above 0.25THz.

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CHAPTER 3

PHASE MATCHING USING BANDGAP STRUCTURES FOR EFFICIENT PARAMETRIC FREQUENCY CONVERSION

3.1 Introduction

Exploiting properties of medium for frequency conversion has been an interesting topic for the past fifty years. This kind of frequency synthesis is commonly achieved using the nonlinearity of the voltage dependent capacitors. The passive harmonics/subharmonics generation is attractive because of better noise performance. These techniques can also be implemented at higher frequencies because cutoff frequency of passive devices is usually higher than active devices [1]. These advantages make passive harmonic/subharmonic generators an ideal candidate for a number of applications including mm-wave and THz imaging [2], spectroscopy [3] and communication [4].

The fundamentals of efficient frequency conversion depend on the phase condition between the input and the parametrically produced output. If ω stands for frequency and k is the phase shift per unit length of a nonlinear transmission line, then

$$\begin{aligned} \omega_3 &= \omega_1 + \omega_2, \\ k_3 &= k_1 + k_2. \end{aligned} \tag{3.1}$$

Above set of equations dictates that in order to produce frequency ω_3 by the combination of input frequencies ω_2 and ω_1, the phase shift, k_3, of the output signal ω_3 should also be the sum of the phase shift, k_2, and phase shift, k_1, of frequencies ω_2 and ω_1, respectively. In other words, sum of the propagation speed of input frequencies ω_1 and ω_2 must be equal to propagation speed of output frequency ω_3.

The improper phase matching leads to the high conversion losses in the case of harmonic generation. Processes like frequency division in NLTL are not even possible if adequate phase matching is not guaranteed [5].

The dispersion relation of a conventional NLTL, shown in Fig. 3.1(a) under the linear capacitor assumption is [6]

$$\omega^2 = \frac{4\sin^2(\frac{k}{2})}{LC}. \tag{3.2}$$

The plot of (3.2) is shown in fig.3.1(b). The plot and above equation make it clear that it is not possible to have $\omega_2 = 2\omega_1$ if we set $k_2 = 2k_1$ or vice versa. At very low frequencies, phase matching can be achieved because (3.2) can be approximated as a straight line but this limits the maximum possible operating frequency that can be achieved with available components.

For frequency up-conversion, previous works have followed different approaches to improve power at higher harmonics. For example, [1] accumulates more nonlinearity over small space using 2-D lattice which increases the power in higher harmonics but decreases the efficiency; and [7] realized importance of phase matching using small signal analysis but their optimization is strongly dependent on the quality factor and coherent length of transmission line. For down conversion, [5] suggests use of dispersion compensation capacitor but this approach is difficult to generalize for higher frequencies and other nonlinear processes. Hence there has always been a need of a structure that inherently, without any external aid, is capable of providing phase matching. Here, we propose a structure that exhibits frequency bandgap and is able to provide accurate phase matching for any kind of frequency conversion. In optics, photonic crystals which possess similar properties are widely proposed for such nonlinear processes [8]. Over 30 years ago, [9] suggested using the similar technique but their approach required extremely long transmission line with single port for both input and output which makes

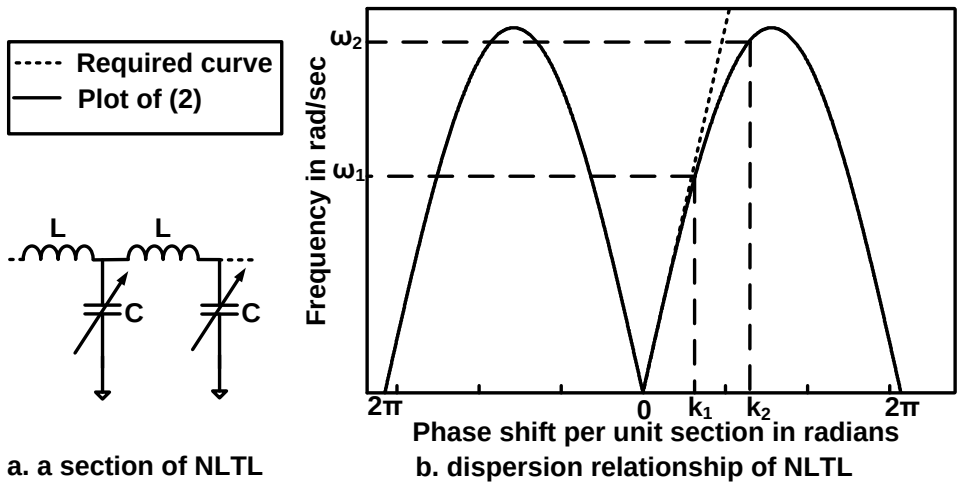

Figure 3.1: Dispersion relationship of discrete transmission line.

their methodology very difficult to use in practical applications.

The paper is organized as follows: Section II explains the basic idea behind bandgap structures and its analytical treatment. Section III discusses the effect of nonlinearity. Section IV and V present the design, simulation and measurement of a board level frequency doubler prototype.

3.2 Bandgap Structure

Consider a nonlinear transmission line with periodic arrangement of inductors and varactors as shown in Fig. 3.2. If voltage at each varactor is represented by V_n, where n is a positive integer, then by applying KCL at node n we can write the following set of equations for every unit cell consisting of L_1C_1 and L_2C_2.

$$\begin{aligned} \frac{V_{n-1}-V_n}{L_2} - \frac{V_n - V_{n+1}}{L_1} &= \frac{d^2}{dt^2}\left(C_1(V_n)V_n\right), \\ \frac{V_{n-2}-V_{n-1}}{L_1} - \frac{V_{n-1} - V_n}{L_2} &= \frac{d^2}{dt^2}\left(C_2(V_{n-1})V_{n-1}\right). \end{aligned} \tag{3.3}$$

The first order approximation of a nonlinear capacitor is

$$C_i(V) = C_i(0)\,(1 - bV) \tag{3.4}$$

where C_i is the capacitance at zero bias, b is the slope of C/V curve and i can be either 1 or 2 since we have varactors of two different values.

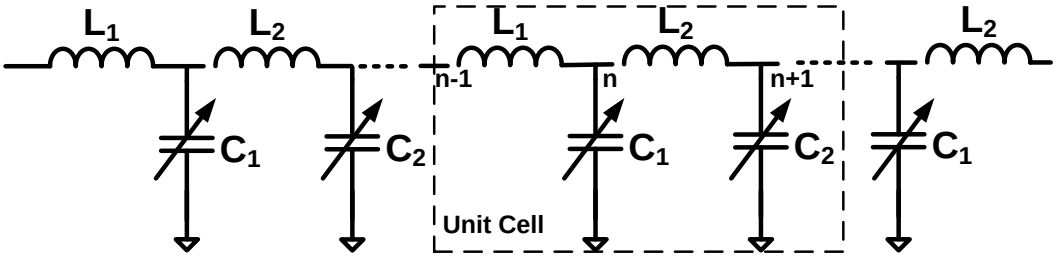

Figure 3.2: Bandgap nonlinear transmission line.

3.2.1 Dispersion Relation

Dispersion relation is derived by assuming the capacitors are linear. If we consider one unit cell consisting of L_1C_1 and L_2C_2, then

$$\omega^2 = \frac{X \pm \sqrt{X^2 - 4Y}}{2}, \tag{3.5}$$

where

$$\begin{aligned} X &= \left(\frac{1}{C_1} + \frac{1}{C_2}\right)\left(\frac{1}{L_1} + \frac{1}{L_2}\right) \\ Y &= \frac{4\sin^2\left(\frac{k}{2}\right)}{L_1L_2C_1C_2}. \end{aligned} \tag{3.6}$$

Here, k is the phase shift per unit cell. The dispersion relationship has two different solutions corresponding to two passbands. The plot of (3.5) is shown in Fig. 3.3. It

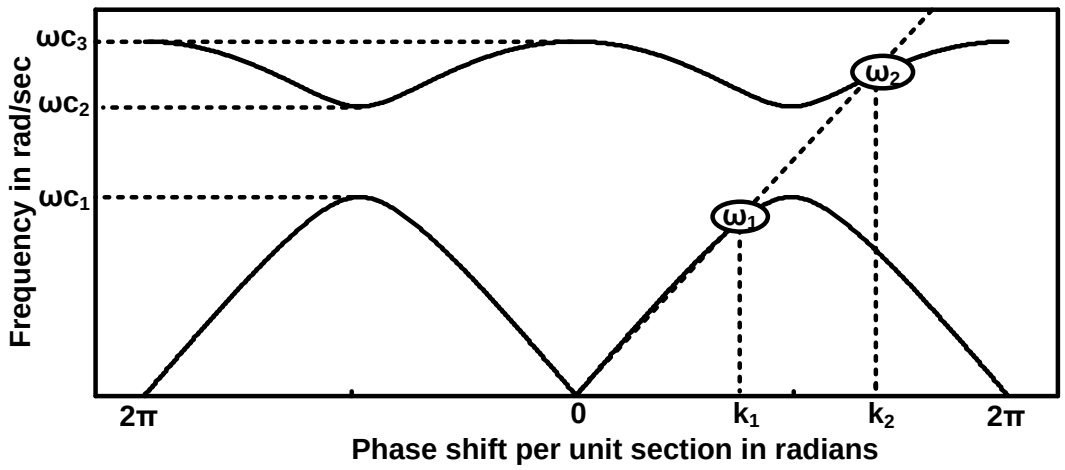

Figure 3.3: Dispersion diagram of a bandgap structure.

has two frequency passbands and a bandgap between them. The position of these passbands can be adjusted by using different parameters. The difference between values of inductors and/or capacitors defines the width of bandgap. If the difference is zero, the bandgap vanishes and this structure transforms into conventional NLTL.

In order to understand phase matching in these structures, consider ω_1 and ω_2 in Fig. 3.3 for frequency doubling application. In order to satisfy, $k_2 = 2k_1$, the second passband is positioned such that $\omega_1 = 2\omega_2$ or vice versa. The second passband can be easily moved upwards and downwards by changing the difference between inductors/varactors values. Hence, these structures can easily satisfy phase matching condition due to the existence of the bandgap. Similarly phase matching can be obtained for frequency dividing or other kinds of parametric frequency conversion.

3.2.2 Bragg Cutoff Frequencies

The cutoff frequency of each passband, as marked in Fig. 3.3, can be calculated from (3.5). The cutoff of the first passband occurs when $k = \pi$ and is given by

$$\omega_{c1} = \sqrt{\frac{X - \sqrt{X^2 - \frac{4}{L_1 L_2 C_1 C_2}}}{2}} \tag{3.7}$$

where X is shown in (3.6). The cutoff of second passpand happen when $k = \pi$ and $k = 0$.

$$\omega_{c2} = \sqrt{\frac{X + \sqrt{X^2 - \frac{4}{L_1 L_2 C_1 C_2}}}{2}} \tag{3.8}$$

$$\omega_{c3} = \sqrt{\left(\frac{1}{C_1} + \frac{1}{C_2}\right)\left(\frac{1}{L_1} + \frac{1}{L_2}\right)} \tag{3.9}$$

If the difference between values of inductors and varactors approaches zero, (3.9) approaches $2/\sqrt{LC}$ which is the bragg cutoff frequency of conventional discrete transmission line shown in (3.2).

3.2.3 Characteristics Impedance of Passbands

One of the interesting properties of bandgap structure is its impedance in two passbands. Here, we are not writing the mathematical form of impedance but we show them graphically in Fig. 3.4. It shows that the real part of impedance of the first passband is higher than that of second passband and is constant over a broad range of frequency, while impedance of second passband is much lower and is narrow band. The circuit parameters can be chosen properly to keep the imaginary part of impedance zero in passbands. Moreover, the unit cell is not symmetric, hence the impedances seen can be different at input port and output port. From the above analysis, it is concluded that

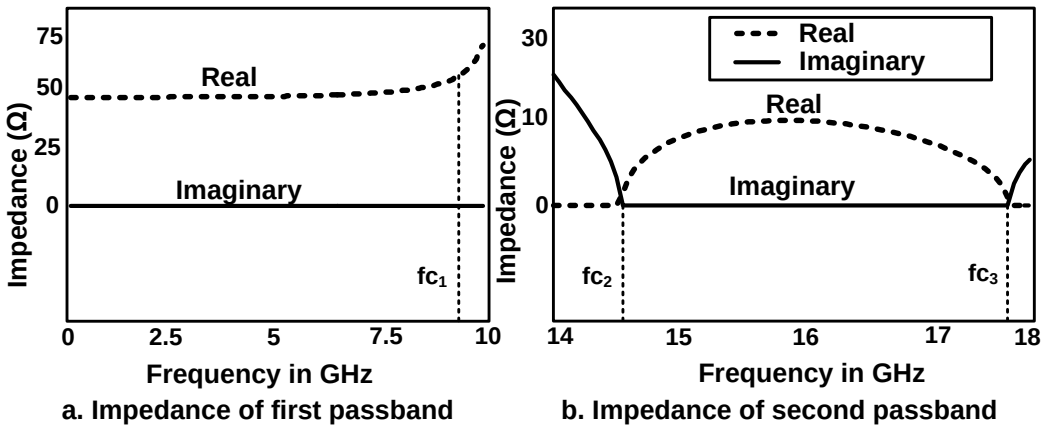

Figure 3.4: Impedance of a bandgap structure in different passbands. $C_1 = C_2 = 500fF$ and $L_1 = 500pH, L_2 = 1nH$.

1. It is very difficult to match bandgap structures for both passbands. So matching should be done accordingly, for example, in order to design frequency doubler one can match input for fundamental frequency and output for second harmonic.
2. Even in the absence of any loss, an asymmetric bandgap structure results in different amplitude of voltages across C_1 and C_2.
3. The same input power results in different voltage amplitudes in passbands because of different characteristics impedance.

3.3 Effect of Nonlinearity

In order to understand the effect of nonlinearity in a bandgap structure, (3) can be written as

$$V_n = \left(\frac{L_1}{L_1+L_2}\right)V_{n-1} + \left(\frac{L_2}{L_1+L_2}\right)V_{n+1} - \left(\frac{L_1L_2}{L_1+L_2}\right)\frac{d^2}{dt^2}\left(C_1(V_n)V_n\right),$$
$$V_{n-1} = \left(\frac{L_2}{L_1+L_2}\right)V_{n-2} + \left(\frac{L_1}{L_1+L_2}\right)V_n - \left(\frac{L_1L_2}{L_1+L_2}\right)\frac{d^2}{dt^2}\left(C_2(V_{n-1})V_{n-1}\right). \quad (3.10)$$

By using the first order approximation of voltage dependent capacitor (3.4), we can write

$$V_n = \left(\frac{L_1}{L_1+L_2}\right)V_{n-1} + \left(\frac{L_2}{L_1+L_2}\right)V_{n+1} + \frac{C_1L_1L_2}{L_1+L_2}\left(\left(\frac{d}{dt}V_n\right)\left(\frac{d}{dt}V_n\right) - \left(\frac{d^2}{dt^2}V_n\right)\right),$$

$$V_{n-1} = \left(\frac{L_2}{L_1+L_2}\right)V_{n-2} + \left(\frac{L_1}{L_1+L_2}\right)V_n + \frac{C_2L_1L_2}{L_1+L_2}\left(b\left(\frac{d}{dt}V_{n-1}\right)\left(\frac{d}{dt}V_{n-1}\right) - \left(\frac{d^2}{dt^2}V_{n-1}\right)\right). \tag{3.11}$$

Clearly, the second last term on the right hand side of (3.11), shows that input signal is mixing with itself. This kind of mixing is the result of nonlinearity in capacitance thus producing second harmonic from the input signal. We numerically solve the system

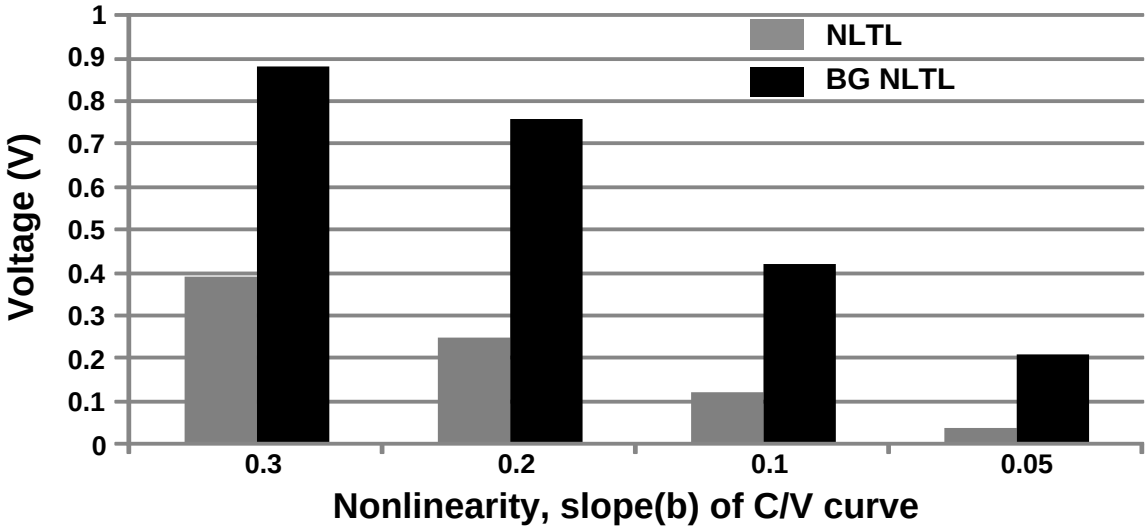

Figure 3.5: Numerical simulation of NLTL and bandgap structure for the fundamental frequency of 8GHz. For NLTL:$C = 500fF$, $L = 725pH$, bragg cutoff = 17GHz. For bandgap NLTL: $C_1 = C_2 = 500fF$ and $L_1 = 500pH, L_2 = 1nH$, upper bragg cutoff = 17GHz.

of nonlinear differential equations (3) for the bandgap NLTL and conventional NLTL in MATLAB. Fig. 3.5 shows comparison between amplitudes of second harmonic of both transmission lines with decrease in nonlinearity. Since, each section of bandgap structure contains twice as many components as in NLTL, we probe voltage amplitude at 5^{th} section of bandgap structure and 10^{th} section of NLTL. The input amplitude is

1V and the bragg cutoff is the same for both structures. Not only bandgap structure produces higher amplitude, it also performs better even with lower nonlinearity.

3.4 Design and Simulation of Frequency Doubler Prototype

A board level prototype for the frequency doubler application is built to convert 175MHz to 350MHz. The k chosen for fundamental frequency and second harmonic is $2\pi/3$ and $4\pi/3$, repectively. The upper cutoff frequency of bandgap NLTL is kept around 400MHz which is very close to second harmonic. After deciding these design specifications, (5) and the parameters of available discrete components are used to determine the values of inductors and varactor diodes. The varactors are kept the same while the difference is introduced in the values of inductors. We use air core inductors of 26nH and 56nH from CoilCraft and varactor diode having 11pF capacitance at 2.2V bias from Panasonic. The diodes are used in the reverse biased configuration.

The Agilent Design System (ADS) is used for the simulation of the prototype. The models of all the components are made using the datasheets provided by vendors. The frequency doubler consists of only five sections of bandgap unit cell. Since, the impedance of both bands are different as shown in previous sections, it is designed to be 50Ω at the input port for the fundamental frequency, while a matching network is used to match the output for second harmonic. The phase plot, Fig. 3.6, shows that phase matching at 175MHz and 350MHz is satisfied. Fig. 3.7 shows the simulated conversion loss and output power against different values of input power at the input signal of 175MHz. The best conversion loss achieved is 4.5dB.

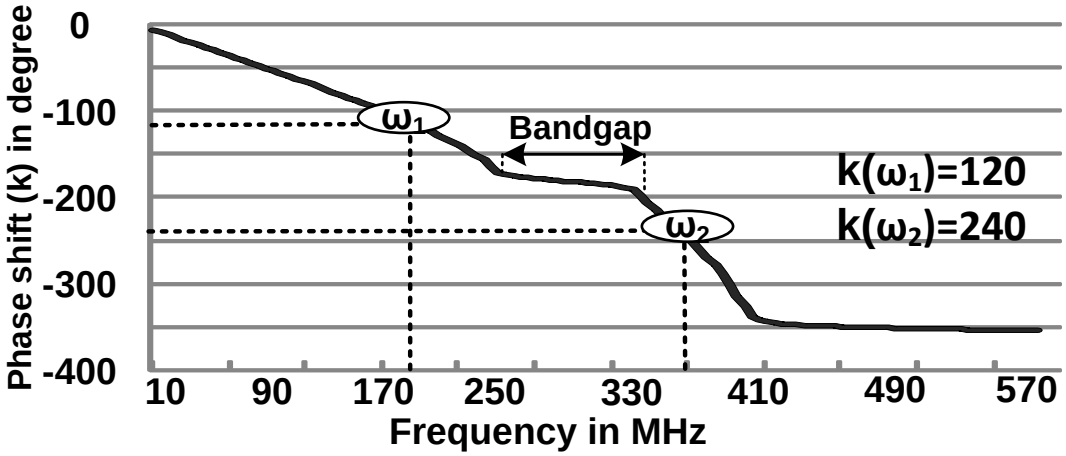

Figure 3.6: Simulated phase shift per unit section vs. frequency.

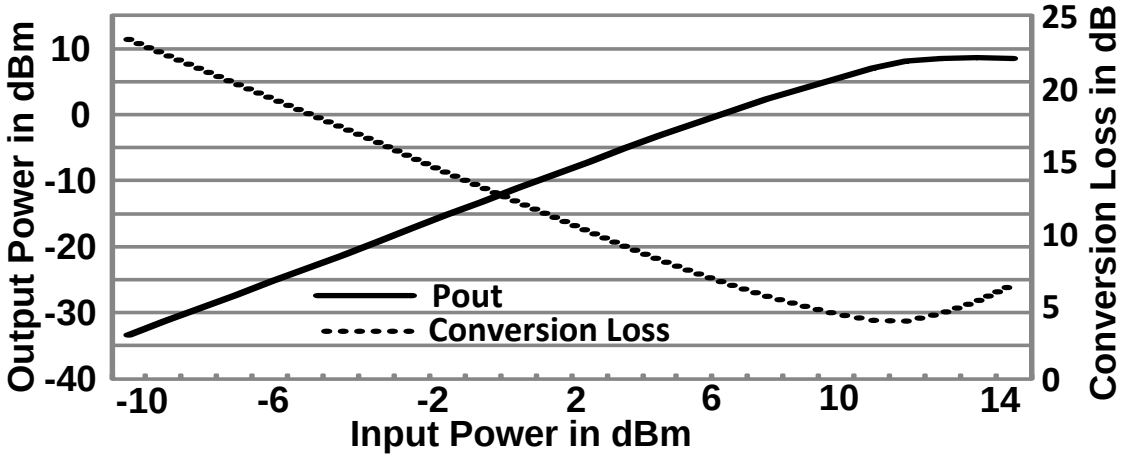

Figure 3.7: Simulated conversion loss and output power vs. input power.

3.5 Measurement Results

Fig. 3.8 shows our frequency doubler prototype. It is measured using a tunable signal source, HP 83623A and a power spectrum analyzer, HP591A. Fig. 3.9 shows that the center frequency of the doubler changes from 146MHz to 156MHz by tuning the reverse bias voltage of the varactor diodes from 2.2V to 2.6V. The optimal fundamental

frequency is shifted from simulated 175MHz to 150MHz. This happens because of the inaccurate component models based on datasheets and the unmodeled PCB parasitics. Fig. 3.10 shows the measured conversion loss and output power against different values of input power. The best conversion loss achieved is around 4.9dB, which is close to our simulation.

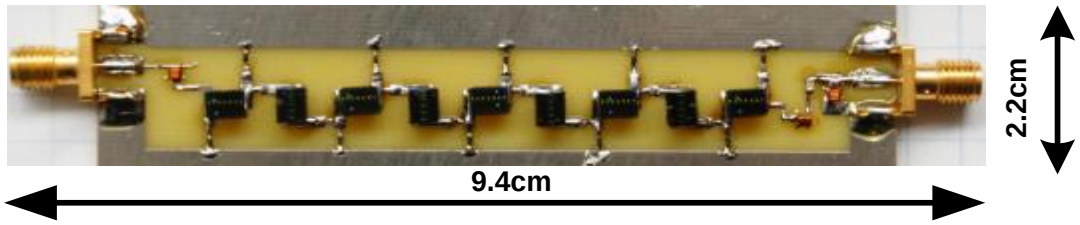

Figure 3.8: Prototype frequency doubler board.

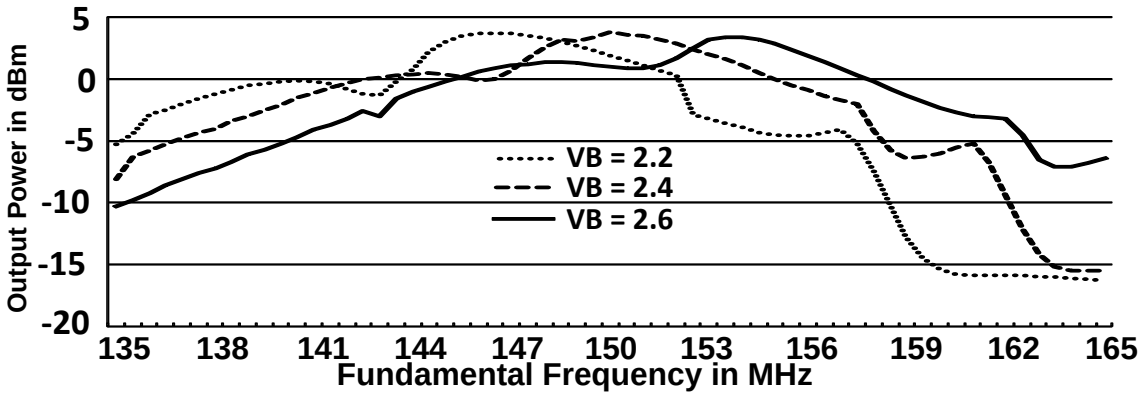

Figure 3.9: Measured output power vs. frequency for input power of 9dBm.

3.6 Conclusion

Parametric frequency conversion is an ideal method for number of applications because of better noise performance, zero DC power consumption and the feasibility of imple-

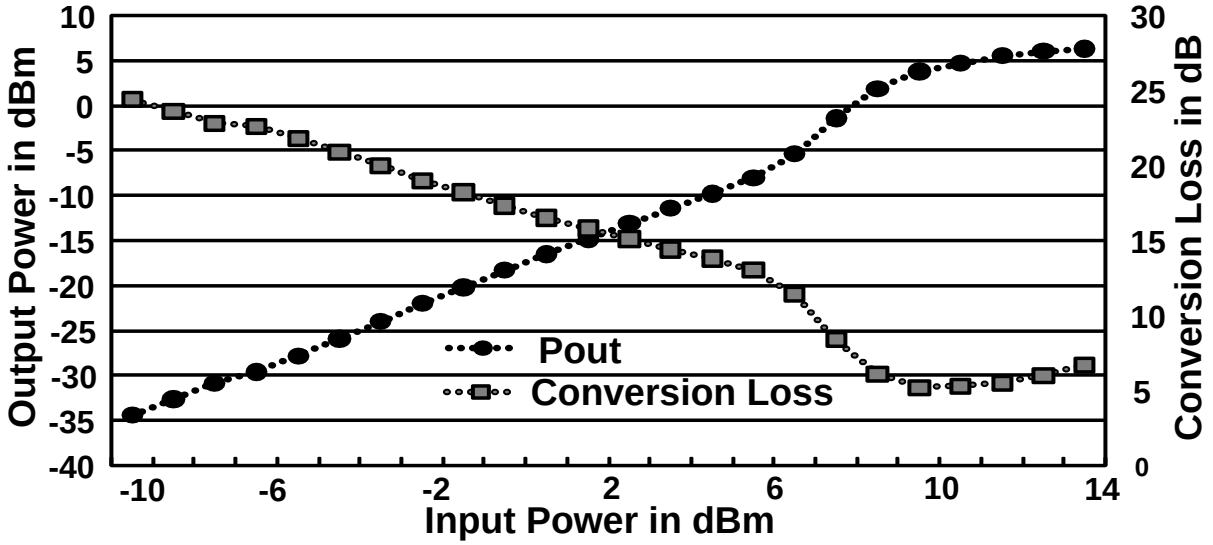

Figure 3.10: Measured output power and conversion loss vs. input power.

mentation at high frequencies. In this paper, by introducing a nonlinear bandgap transmission line, we proposed a structure that could provide accurate phase matching for parametric frequency conversion as compared to the existing NLTL, which is bulky and inefficient. Meanwhile, this structure is also compatible with CMOS technologies that may find its applications in on-chip high-frequency parametric processes.

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CHAPTER 4

MICROWAVE & MM-WAVE FREQUENCY MULTIPLIERS USING NONLINEAR PASSIVE RESONATOR TECHNIQUE.

4.1 Introduction

High frequency signal generation is very interesting [1] because of the emerging mm-wave and sub mm-wave applications including vehicular radars, short range communication, broadband wireless access such as WiMax, imaging and spectroscopy [2], [3], [4], [5], [6]. The oscillators employed for high frequency generation are theoretically limited by the cutoff frequency, f_{max}, of active devices. The fundamental oscillation frequency achieved is usually much less than the reported f_{max} of transistors because of the substrate losses, low quality factor of passive devices and difficulty to meet the optimal loading requirements of active elements, [7]. Moreover achieved power levels are not adequate for high frequency applications. Moreover high frequency oscillators are difficult to tune. To achieve tunable and high frequency synthesis, usually frequency multipliers are employed. The frequency multipliers can be generally classified as active or passive.

There are many variants of active multipliers. Injection locking based frequency synthesizers can usually operate with lower input power at the center frequency. However, their phase noise degrades with increase in the offset frequency[8]. Also they have limited. Another class of active multipliers rely majorly on the nonlinearity of active devices such as transistors. These synthesizers are broadband but they dissipate more DC power and require high input power levels. The passive multipliers rely on the nonlinearity of the passive device, usually voltage dependent capacitors called varactors. The varactors have high cutoff frequency and give better noise performance. These ad-

vantages enable passive frequency synthesizers to operate at high frequencies and make them good candidate for mm-wave and THz applications.

In this paper, we focus on nonlinear transmission lines (NLTL) based structures, that are famous for broadband harmonic generation. NLTLs are capable of implementing other interesting phenomenon too. Earlier, pulse shaping and soliton generation in a 1-D NLTL is shown in [9]. Recently, [10] shows even sharper and higher amplitude soliton pulses using 2-D NLTL medium. NLTLs also have the potential of generating sub-harmonics, [11] exploits parametric amplification and demonstrates frequency division using phase sensitive gain offered by a phase matched NLTL. The phase sensitive gain via NLTL has been studied to provide noise squeezing, [13] [12]. The 2-D nonlinear lattice has also been shown as a feasible alternative for high quantization [14]. A 2-D lattice is also shown to perform interesting analog signal processing computations such as Fourier transform, [15].

In this work, we focus on a nonlinear transmission lines (NLTLs) based frequency multipliers. An NLTL consists of a series of inductors periodically loaded with voltage dependent capacitors called varactors. These structures are limited by two factors: i) dispersion ii) high input power. Dispersion refers to the phenomenon in which propagation velocity varies with the change in frequency. It is the property of discretness, hence cannot be avioded [17] in discrete transmission line structures. Moreover, it gets worse with increase in frequency. To overcome dispersion, we introduce an alternate approach based on a bandgap structure. A bandgap structure effectively decouples the propagation constant of the input and output frequencies. To relax the input power requirement and decrease die area, we propose resonator approach with active loading. As a proof of concept, we build a frequency doubler at 20GHz in a 65nm CMOS process [21]. The doubler takes single ended input and provides differential output with the

conversion loss of 3.5dB at 3dBm of input power. We extend the proposed methodology for multiply-by-three applications. In order to show the feasibility of our approach near f_{max}, a 100GHz frequency tripler is implemented in a 130nm process. The frequency tripler is tested from 85GHz to 120GHz and it provides conversion loss of around 12dB with the input power of 8dBm. The relative bandwidth of doubler and tripler is about 23% and 12.3%. The frequency tripler outperforms any previously reported work in terms of output power and 3dB bandwidth at the same technology node.

The rest of the paper is organized as follows: section II contains the analytical treatment of homogeneous NLTL. Based on the analysis, we quantify effects of dispersion on second and third harmonic generation. Section II also proposes bandgap NLTL to compensate for dispersion. Section III discuses the design and implementation of frequency doubler. Section IV, describes the design methodologies, simulation and measurement results of frequency tripler. Section V concludes the paper.

4.2 A nonlinear transmission line based frequency multipliers

The fundamentals of efficient nonlinear frequency conversion depend on the phase matching condition,[18], between the inputs and outputs. If ω stands for frequency and β is the phase shift per unit length of a nonlinear transmission line, then

$$\begin{aligned} \omega_3 &= \omega_1 + \omega_2, \\ \beta_3 &= \beta_1 + \beta_2. \end{aligned} \tag{4.1}$$

Above set of equations dictates that in order to produce ω_3 by the nonlinear interaction of ω_2 and ω_1, the phase shift, β_3, of the ω_3 should be the sum of the phase shifts β_2, and β_1, of frequencies ω_2 and ω_1, respectively. In other words, sum of the propagation speed of input frequencies ω_1 and ω_2 must be equal to propagation speed of output frequency

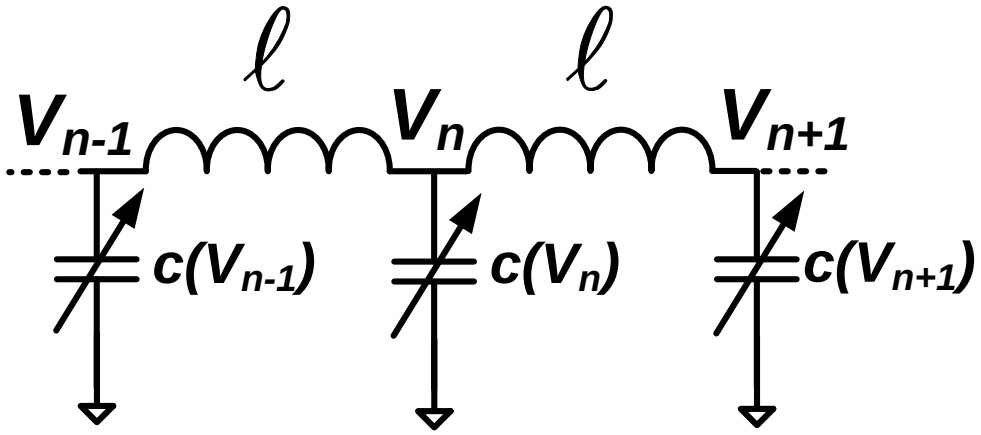

Figure 4.1: A homogeneous nonlinear transmission line.

ω_3. In the presence of dispersion, the input frequency components does not maintain their original phase relationships as they propagate, [19].

4.2.1 A homogeneous nonlinear transmission line

Fig. 4.1 shows a nonlinear transmission line (NLTL), consisting of inductors l and voltage dependent capacitors $c(V)$. If voltage at each capacitor is V_n, where n is the section number, then by applying KCL at node n and KVL across the two adjacent inductors, we obtain [20]

$$V_{n-1} - 2V_n + V_{n+1} = l\frac{d^2}{dt^2}(c(V_n)V_n) \tag{4.2}$$

The nonlinear capacitance is represented using first-order approximation as

$$c(V) = c_0\,(1 - bV) \tag{4.3}$$

where c_0 is the capacitance at zero bias and b is the slope of the c/V curve. We can transform (4.2) in to a PDE by introducing variable h, spacing between adjacent nodes.

If $V_n = V(nh) \simeq V(x)$, $L = l/h$ and $C = c/h$ then

$$\frac{\partial^2 V(x)}{\partial x^2} = L\frac{\partial^2}{\partial t^2}(C(V)V(x)). \tag{4.4}$$

Substituting (4.3) in to (4.4), we have

$$\frac{\partial^2 V(x)}{\partial x^2} = LC_0\frac{\partial^2}{\partial t^2}(V(x)) + LC_0 b\frac{\partial^2}{\partial t^2}(V(x)V(x)). \tag{4.5}$$

Last term of (4.5) predicts the second harmonic generation by self-mixing of signal through a nonlinear process

Now consider a case, where this structure has single-tone input with frequency ω_i and propagation constant β_i. This input generates second harmonic with frequency ω and propagation constant β. We further assume that the cutoff frequency of NLTL is between 2$^{\text{nd}}$ and 3$^{\text{rd}}$ harmonic, hence only fundamental and second harmonic can propagate. These assumptions lead to following boundary conditions:

$$\begin{aligned} V_1(x) &= \frac{A_1}{2}\left(e^{j(\omega_i t-\beta_i x)} + e^{-j(\omega_i t-\beta_i x)}\right), \\ V_2(x) &= A(x)e^{j(\omega t-\beta x)} + A(x)^* e^{-j(\omega t-\beta x)}, \\ V(x) &= V_1(x) + V_2(x), \\ V_2(0) &= 0. \end{aligned} \tag{4.6}$$

In (4.6), $V(x)$ represents voltage at any point x on the transmission line and is combination of first harmonic $V_1(x)$ and second harmonic $V_2(x)$. A_1 is the input amplitude of first harmonic and A represents the amplitude of second harmonic. The last equation in (4.6) dictates that there is no second harmonic injected at the input of the line.

4.2.2 Perfect Phase Matched Solution

Perfect phase matching for second harmonic generation means the propagation velocity of 2^{nd} harmonic is exactly same as the propagation velocity of fundamental. In other words

$$\begin{aligned} \omega &= 2\omega_i, \\ \beta &= 2\beta_i = \omega\sqrt{LC_0}. \end{aligned} \tag{4.7}$$

applying (4.6) and (4.7) in to (4.5), following coupled mode equation can be derived.

$$\begin{aligned} \frac{\partial A(x)}{\partial x} &= \frac{-j\beta b A_1^2}{8} \\ \frac{\partial A(x)^*}{\partial x} &= \frac{j\beta b A_1^2}{8} \end{aligned} \tag{4.8}$$

Using above we can write

$$A(x) = \frac{\beta b x A_1^2}{8}$$

and approximated amplitude at the nth section is

$$\begin{aligned} A(n) &= \frac{1}{8}A_1^2 bnh\omega\sqrt{\frac{c_0}{h}\frac{l}{h}} \\ &= \frac{1}{8}A_1^2 bn\omega\sqrt{lc_0} \end{aligned} \tag{4.9}$$

where A_1 is the amplitude of fundamental and $A(n)$ is the amplitude of 2^{nd} harmonic at node n.

4.2.3 Effect of Phase Mismatch

Consider a weak dispersion in the transmission line meaning $\beta \neq 2\beta_i$. If $\Delta\beta = 2\beta_i - \beta$ then following the above derivation following solution can be approximated.

$$\begin{aligned} A(x) &= \frac{b\beta A_1^2}{8}.\frac{e^{-jx\Delta\beta}-1}{\Delta\beta} \\ &= -\frac{jxb\beta A_1^2}{8}.\left(e^{-jx\Delta\beta/2}\left(\frac{sin(\Delta\beta x/2)}{\Delta\beta x/2}\right)\right) \end{aligned} \tag{4.10}$$

$$\begin{aligned} A(x)^* &= \frac{b\beta A_1^2}{8}.\frac{e^{jx\Delta\beta}-1}{\Delta\beta} \\ &= \frac{jxb\beta A_1^2}{8}.\left(e^{jx\Delta\beta/2}\left(\frac{sin(\Delta\beta x/2)}{\Delta\beta x/2}\right)\right) \end{aligned} \tag{4.11}$$

By combining (4.10) and (4.11), we can write

$$A(x) = \frac{bx\beta A_1^2}{8}.\left(\frac{sin(\Delta\beta x/2)}{\Delta\beta x/2}\right) \tag{4.12}$$

and for discrete transmission line case

$$A(n) = \frac{bn\beta A_1^2}{8}\left(\frac{sin(\Delta\beta n/2)}{\Delta\beta n/2}\right). \tag{4.13}$$

Similar to (4.9), (4.13) demonstrates that $A(n)$ increases with β and nonlinearity constant b. More importantly, (4.13) shows that even a slight phase mismatch, $\Delta\beta$, degrades the amplitude of second harmonic. We plot the normalized second harmonic amplitude, $\frac{|A(n)|}{|A(n)|_{\Delta\beta=0}}$ as a function of section number for different values of relative phase mismatch in Fig. 4.2.

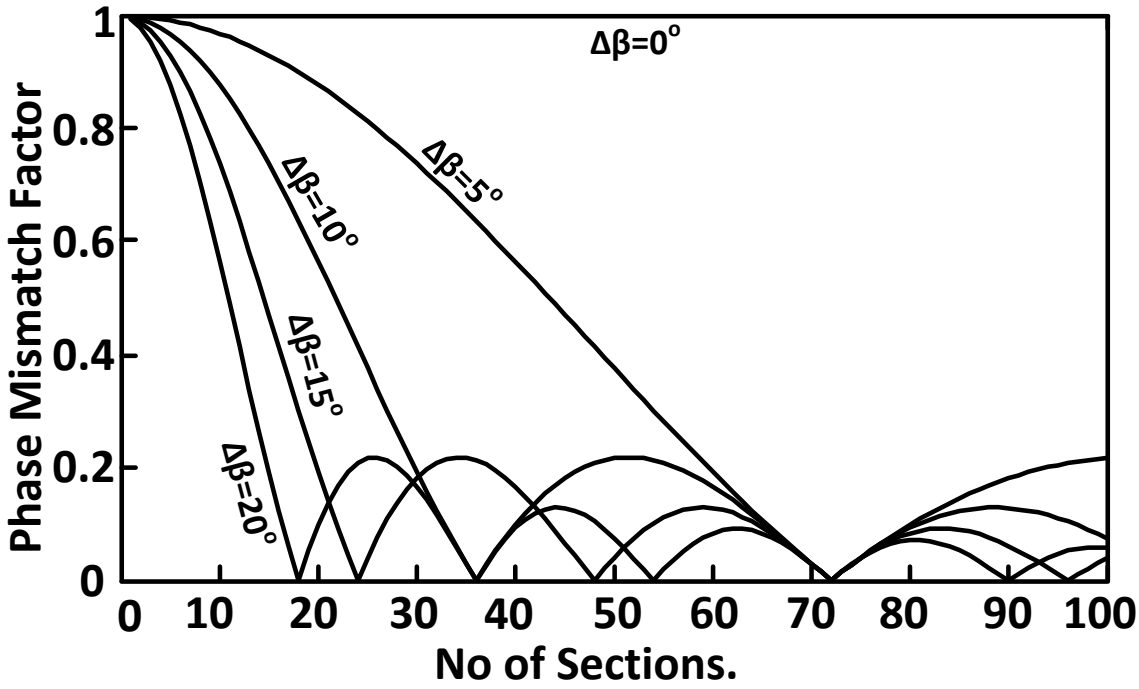

Figure 4.2: The effect of phase mismatch in a homogenerous NLTL.

4.2.4 A bandgap nonlinear transmission line for second harmonic generation

In homogeneous discrete NLTL, dispersion and hence phase mismatch become worse as the frequency approaches cutoff frequency. So for the efficient nonlinear frequency conversion, one has to operate significantly below the cutoff frequency of the line. But at lower frequencies, β is smaller and hence, according to (4.9), large number of sections is required, which translates into large chip area and loss. Also, in a CMOS process, values of inductors and varactors cannot be arbitrarily small due to the parasitics. This limits the cutoff frequency and subsequently the maximum operating frequency of homogenous NLTL.

We solve this problem by decoupling the propagation constants of 1st and 2nd harmonic along the transmission line. This can be performed by periodically changing the values of alternate capacitors and inductors as shown in Fig. 4.3. Such arrangement introduces a bandgap in the dispersion relation that can be engineered by controlling the component values. Assuming linear capacitor the dispersion relation of this structure is given by

$$\omega^2 = \frac{X \pm \sqrt{X^2 - 4Y}}{2}, \tag{4.14}$$

where

$$\begin{aligned} X &= \left(\frac{1}{C_1} + \frac{1}{C_2}\right)\left(\frac{1}{L_1} + \frac{1}{L_2}\right) \\ Y &= \frac{4\sin^2(\frac{\beta}{2})}{L_1 L_2 C_1 C_2}. \end{aligned} \tag{4.15}$$

To intuitively understand phase matching in bandgap structure, we consider plot of its dispersion relation in Fig. 4.3 assuming linear capacitors i.e., $b = 0$. This is clear from Fig. 4.3 that, by tuning bandgap, one can place the fundamental in the first passband and second harmonic in the second passband such that $\Delta\beta = 0$.

The cutoff frequency of each passband, as marked in Fig. 4.3, can be calculated from (4.14). The cutoff of the first passband occurs when $k = \pi$ and is given by

$$\omega_{c1} = \sqrt{\frac{X - \sqrt{X^2 - \frac{4}{L_1 L_2 C_1 C_2}}}{2}} \tag{4.16}$$

where X is shown in (4.15). The cutoff of second passpand happen when $k = \pi$ and $k = 0$.

$$\omega_{c2} = \sqrt{\frac{X + \sqrt{X^2 - \frac{4}{L_1 L_2 C_1 C_2}}}{2}} \tag{4.17}$$

$$\omega_{c3} = \sqrt{\left(\frac{1}{C_1} + \frac{1}{C_2}\right)\left(\frac{1}{L_1} + \frac{1}{L_2}\right)} \tag{4.18}$$

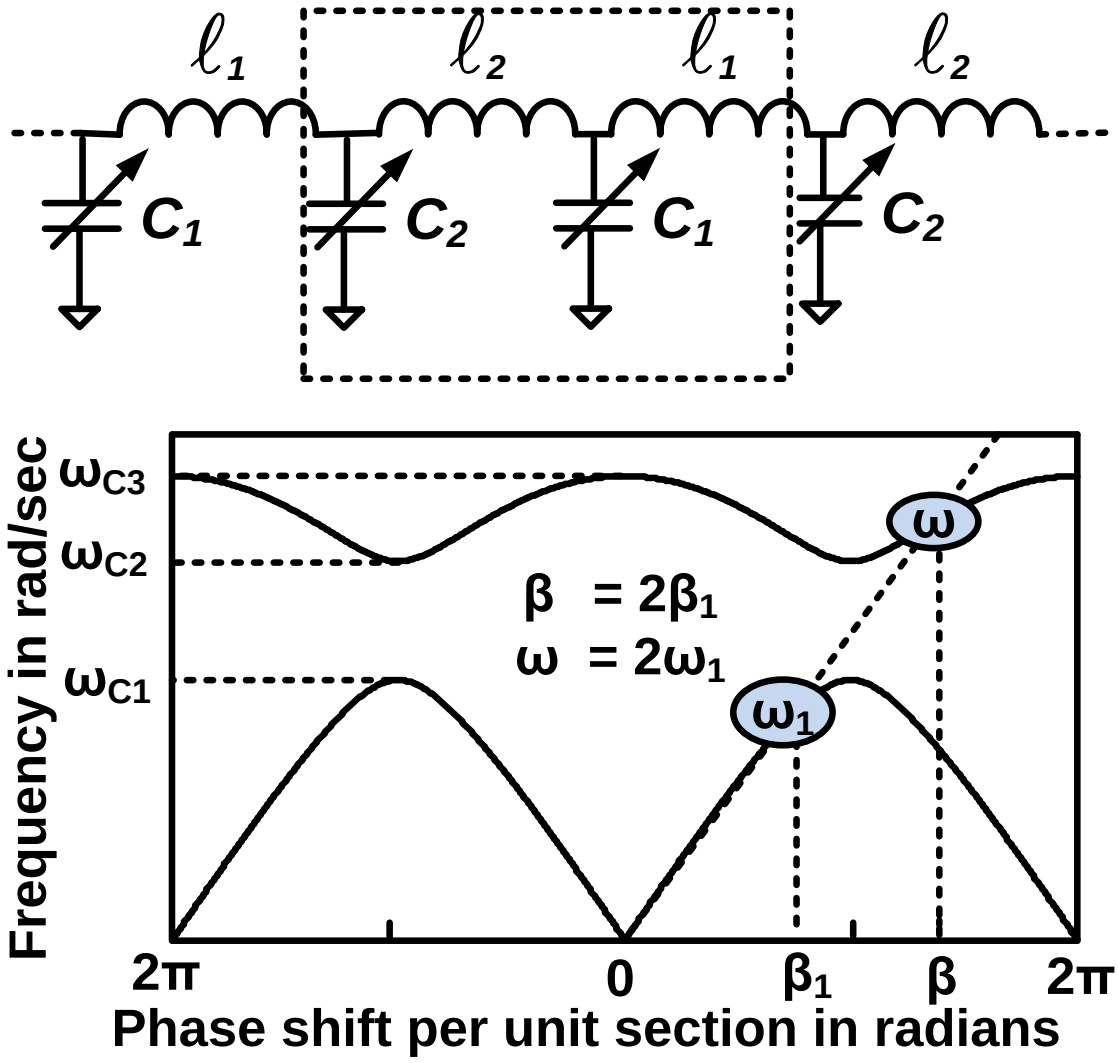

Figure 4.3: Top: The bandgap nonlinear transmission line. Bottom: Dispersion diagram of bandgap structure

If the difference between values of inductors and varactors approaches zero, (4.18) approaches $2/\sqrt{LC}$ which is the bragg cutoff frequency of conventional discrete transmission line.

To demonstrate feasibility of bandgap NLTL for phase matching, we designed a homogeneous NLTL and a bandgap NLTL using ideal components and with same cutoff frequencies as well as nonlinearity constant. The cutoff frequencies of both transmission

lines are less than $23GHz$ and nonlinearity constant is 0.5. The NLTLs are intended to convert $10GHz$ to $20GHz$. Since third harmonic lies beyond the cutoff frequency hence the structure can only propagate fundamental and second harmonic. Fig. 4.4 shows the simulated phase shift per unit section of both transmission lines. It can be seen in Fig. 4.4 that $\Delta\beta = 0$ for bandgap NLTL, however it is 18.6^o in case of homogeneous NLTL.

The input power is 0 dBm for both structures. Fig. 4.5 shows the simulated and analytical amplitude of 2nd harmonic in both lines. The result of homogeneous NLTL matches well with (4.13) and the result of bandgap NLTL confirms (4.9), which is derived assuming perfect phase match.

4.2.5 An extension for efficient third harmonic generation

We can extend the concept of phase matching via bandgap structure for the efficient generation of 3rd harmonic. The CMOS varactor is known to have 2nd order nonlinearity (b_2) along with 1st order nonlinearity. Hence,

$$c(V) = c_0\left(1 + b_1V + b_2V^2\right). \tag{4.19}$$

Using (4.19) we can transform (4.5) in to

$$\frac{\partial^2 V(x)}{\partial x^2} = LC_0\frac{\partial^2}{\partial t^2}(V(x)) + LC_0b_1\frac{\partial^2}{\partial t^2}(V(x)V(x)) + LC_0b_2\frac{\partial^2}{\partial t^2}(V(x)V(x)V(x)). \tag{4.20}$$

(4.19) gives us a very useful insight. There are two distinct ways of 3rd harmonic generation. The last term on the RHS confirms that b_2 can be utilized for the direct conversion of fundamental in to 3rd harmonic. Similarly, according to the second term on RHS, b_1 can be utilized to first generate 2nd harmonic and subsequently 3rd harmonic via nonlinear mixing of fundamental and 2nd harmonic. From (4.19) b_1 and b_2 can be derived

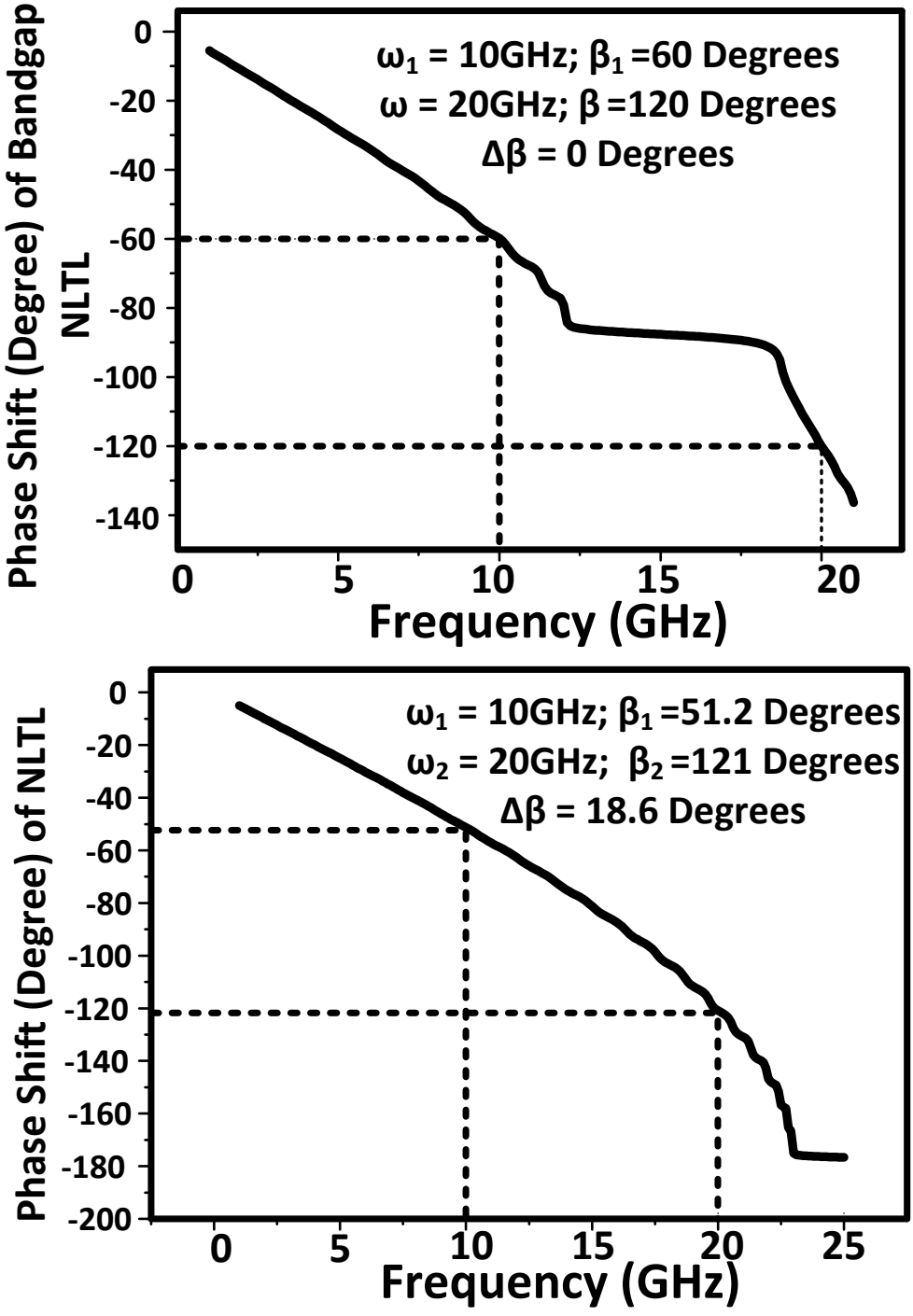

Figure 4.4: Top: phase shift of bandgap transmission line. Bottom: phase shift of homogeneous transmission line

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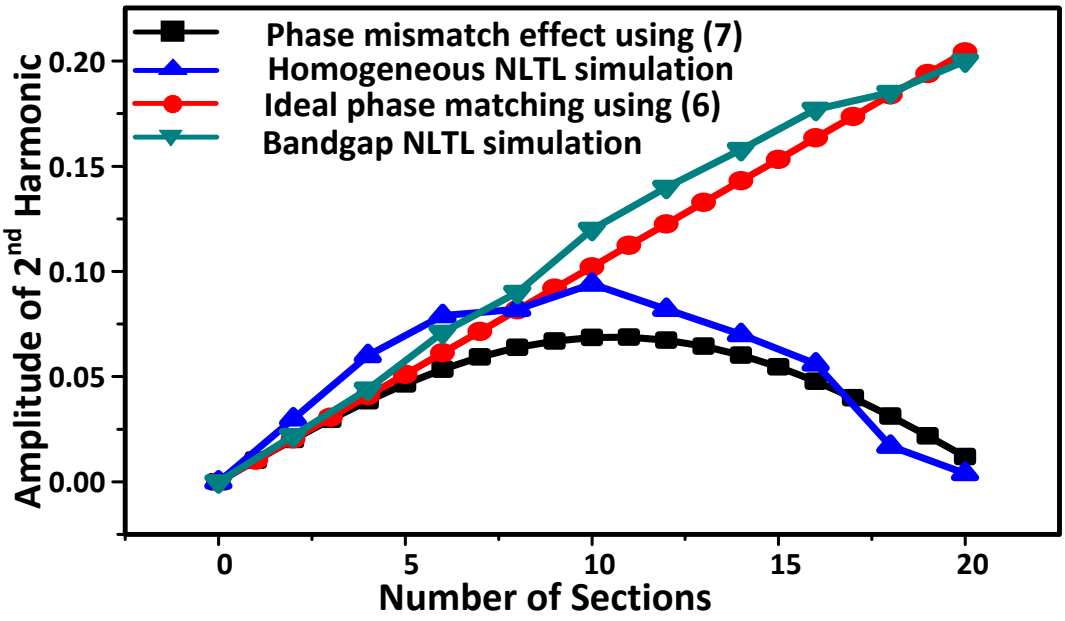

Figure 4.5: Comparison between simulated and analytical results

as

$$b_1 = \frac{1}{c_0}\frac{\partial}{\partial V}(C(V)) - 2b_2V^2 \tag{4.21}$$
$$b_2 = \frac{1}{2c_0}\frac{\partial}{\partial V}(C(V))$$

Here b_1 and b_2 are functions of bias voltage of varactor. Fig. 4.6 shows the capacitance curve of a typical 130nm CMOS varactor along with values of b_1 and b_2 at $100Ghz$. The values of b_1 and b_2 are calculated using (4.21). These curves show that b_1 is maximum around $-0.1V$ and is a even function of voltage across the varactor. However, b_2 switches polarity around $-0.1V$. So if second order nonlinearity (b_2) is utilized, the generated third harmonic from the left half tends to cancel the third harmonic generated in the right half because of the switched polarity. This fact can also be explained

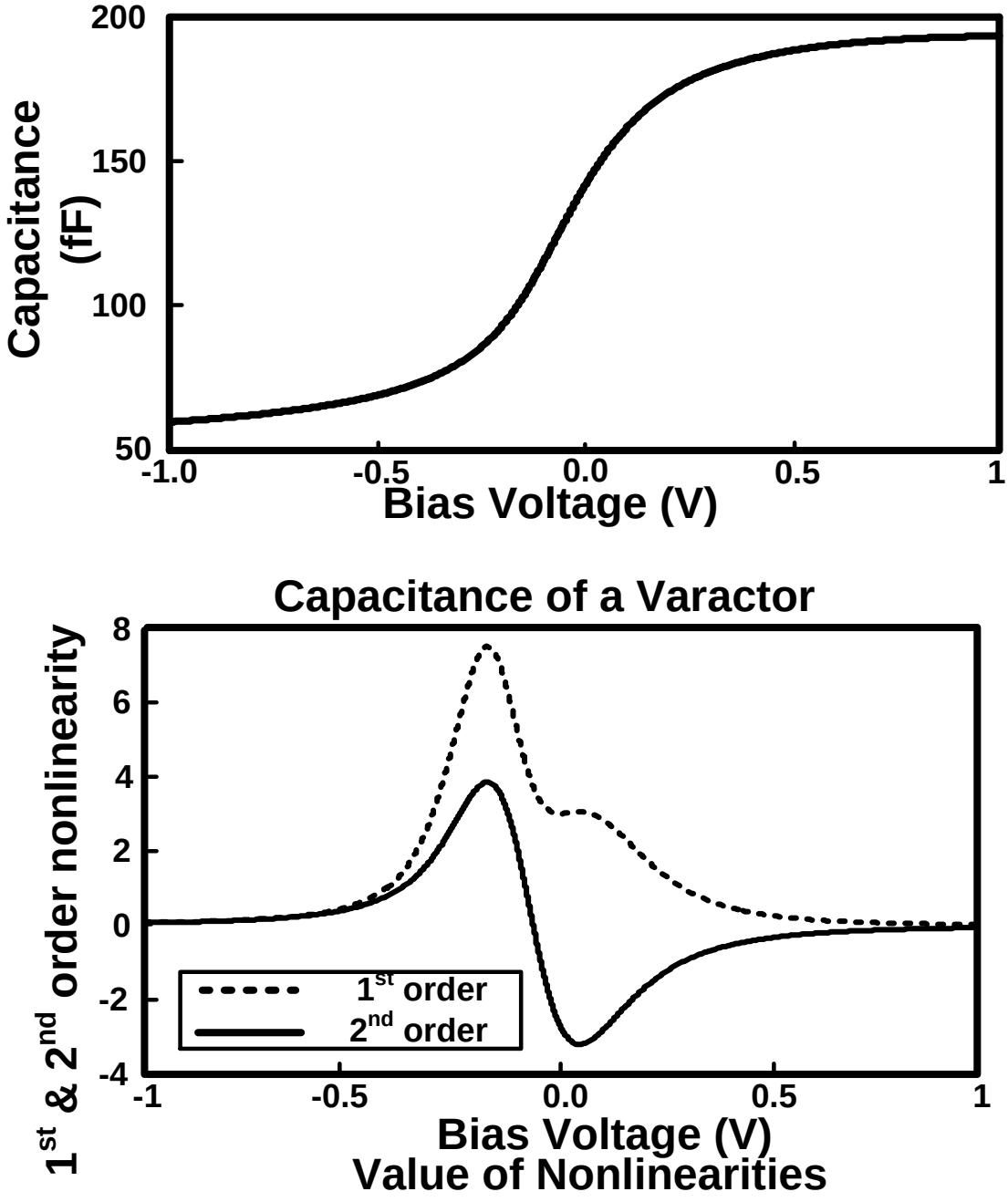

Figure 4.6: Top: capacitance of varactor against bias voltage; Bottom: value of first and second order nonlinearity at various bias voltages.

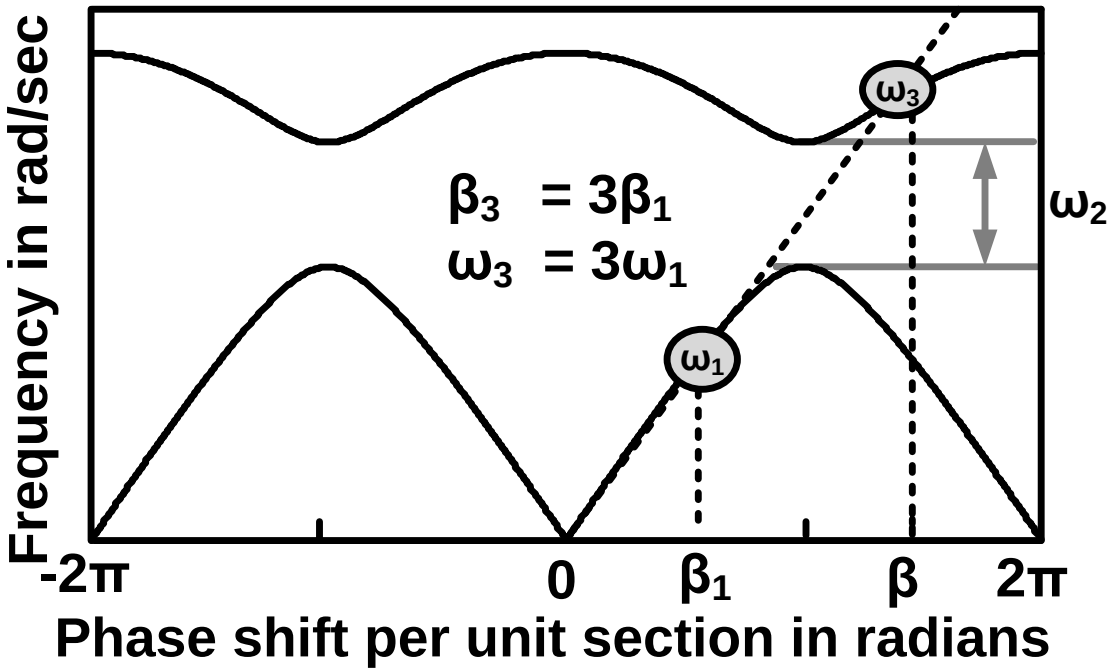

Figure 4.7: Phase matching for multiply-by-three using bandgap structure.

by the average value of b_1 and b_2 i.e. 0.921 and -0.01 respectively. Other than the argument presented, importance of idlers for efficient frequency multiplication/division by three using varactors is analytically investigated in literature, [22][23][24].

From above discussion, it is feasible to use indirect third harmonic generation using first order nonlinearity (b_1) which implies phase matching is needed at two different levels. Using bandgap structure, one can place first harmonic in the first passband and third harmonic in the second passband by making sure that second harmonic lies in the stop band as shown in Fig. 4.7. This placement of harmonics does not support propagation of second harmonic that implies it is trapped forming a standing wave within each section of bandgap transmission line.

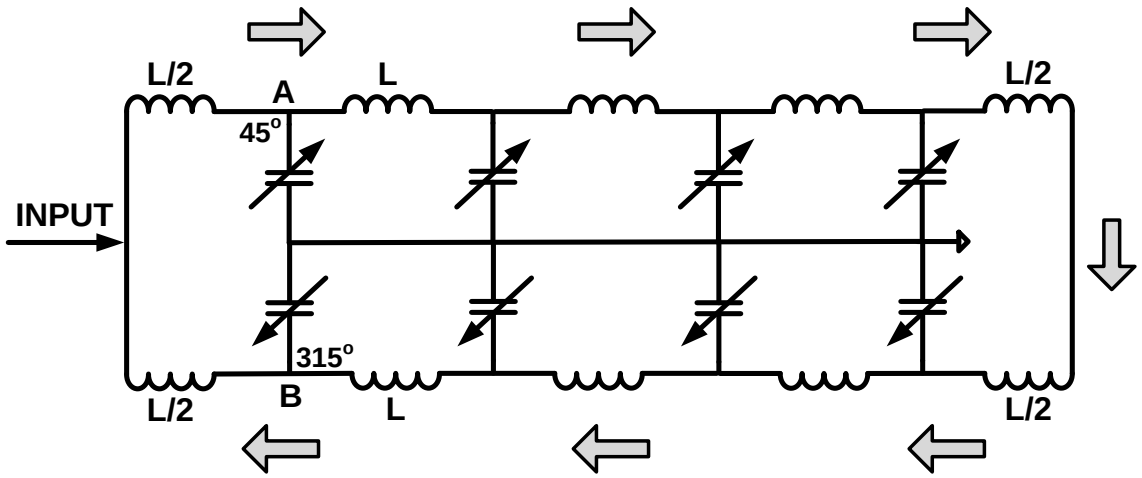

Figure 4.8: Resonator design for frequency doubler

4.3 Design and Measurement of Frequency Doubler

4.3.1 A tapered resonator for differential operation

In order to relax the input power requirement and decrease chip size, a resonator approach is adopted. In case of frequency doubler, an aasymetric resonator is design in a such a way that the structure takes single ended input and generates differential output without any explicit balun or polyphase filter.

Fig. 4.8 shows a proposed resonator structure. Fig. 4.8 shows desired phase difference of fundamental with respect to input at point A and point B. The second harmonic at any two points on the resonator will be differential with respect to each other only if the phase difference of fundamental between these two points is either $\pi/2$ or $3\pi/2$. We require unidirectional wave propagation to generate differential output. Since the phase difference between A and B is 270 degree, the second harmonic generated at these two points will be differential with respect to each other.

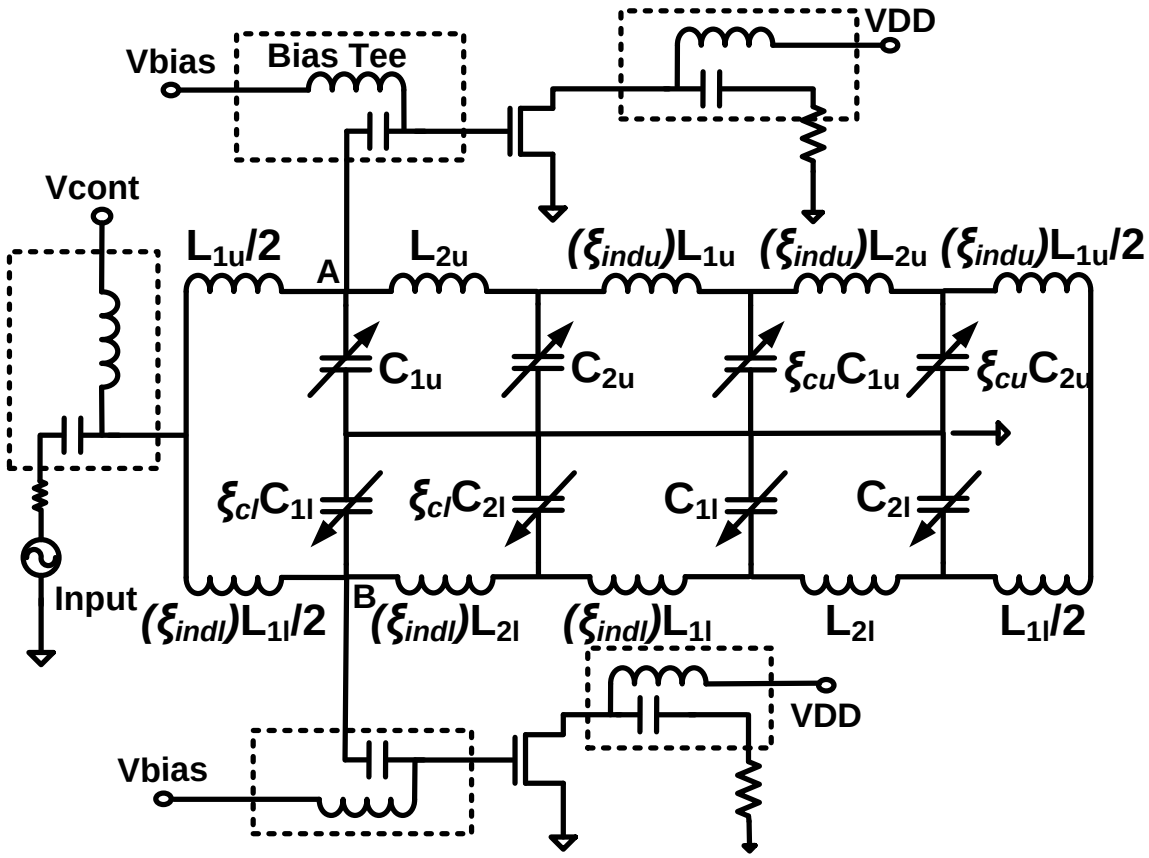

Figure 4.9: Schematic of Frequency Doubler

The implementation of unidirection resonator using bandgap structure is challenging. To enforce unidirectional flow, we choose different impedance of the top transmission line compared to bottom transmission line. For smooth propogation, we taper resonator such that L/C increases in the direction of propagation (Fig. 4.9).

Another challenge is to take the output from the resonator. The resistive loading lowers the quality factor of resonator. We employ capacitive loading and use buffers to load the resonator. The capacitance of buffers is absorbed inside the resonator itself.

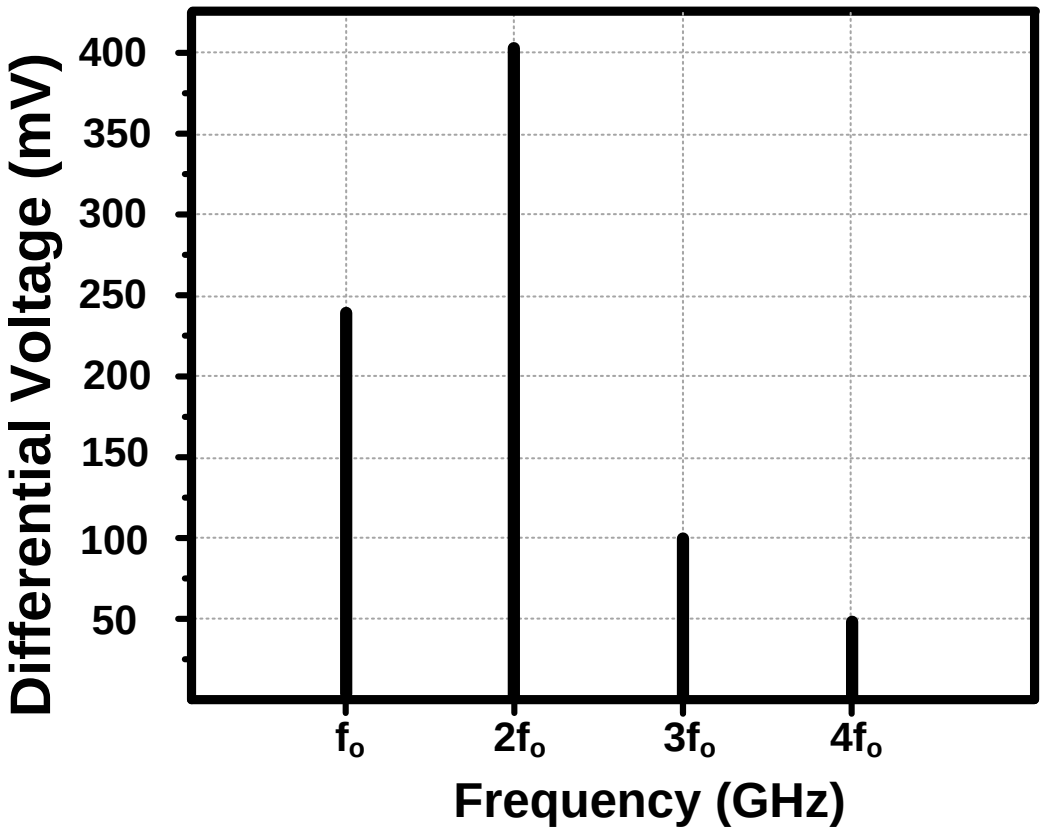

Figure 4.10: differential voltage amplitude of 1st and 2nd harmonic.

4.3.2 Simulation & Measurement Results

We build a doubler prototype using the priciple described above in a TSMC 65nm CMOS process. The input frequency is kept to be around 10GHz and the cutoff frequency of transmission structure is 25GHz. The input of doubler is matched to 50Ω without any matching network. The measurement is done using a signal source (HP83623A) and a spectrum analyzer (HP859A). The input matching is confirmed using Agilent E8364B network analyzer.

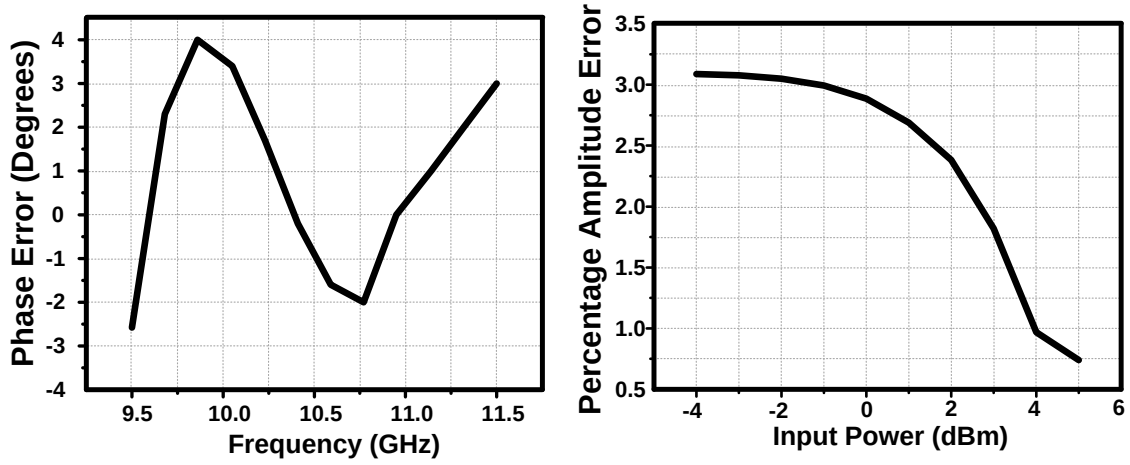

Figure 4.11: Phase error and amplitude error

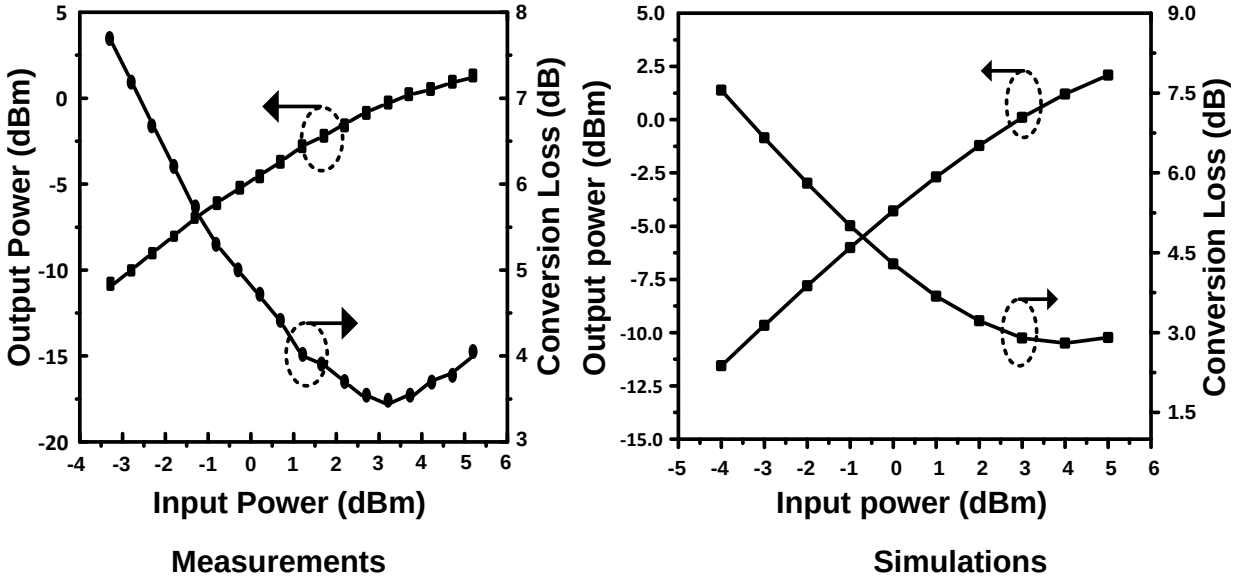

Figure 4.12: Conversion loss and output power against various input powers.

Fig. 4.10 shows differential voltage amplitude of 1st and 2nd harmonic at point A and B for the input power of 3dBm. Fig. 4.11 shows the amplitude error and phase error between differential output. The phase error is less than 5^o and amplitude error decrease with the increase in input power.

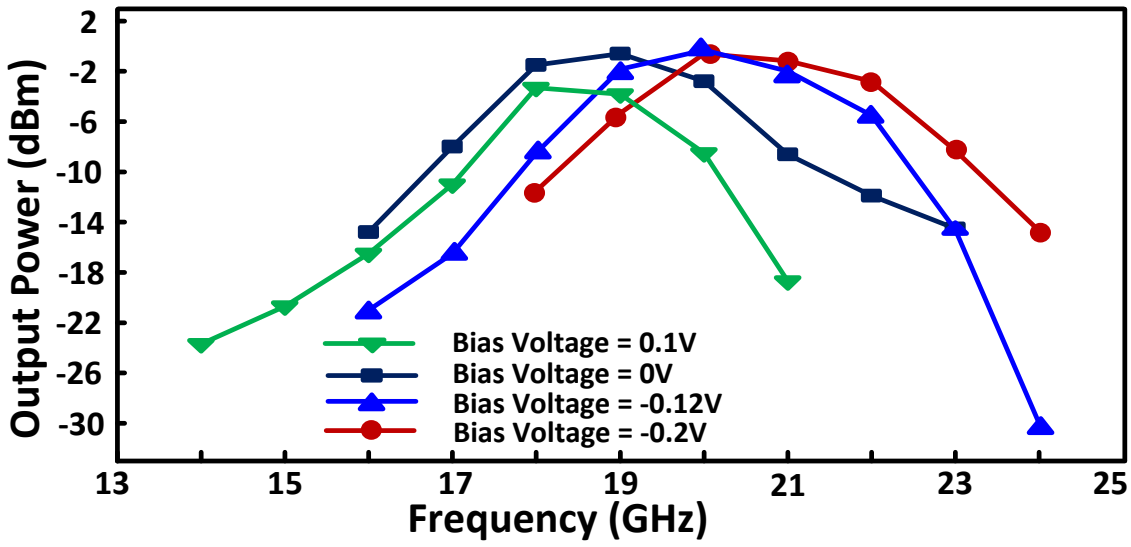

Figure 4.13: Tuning nature of resonator

Fig. 4.12 shows the conversion loss and output power against various input powers. The best conversion loss we achieve is -3.5dB. Moreover, the conversion loss remains very good even at the very low input powers. Even at -3dbm of input power, the conversion loss is around -7.6dB. Fig. 4.13 shows the tunability of this frequency doubler at the input power of 3dBm.

The tuning is performed by changing the bias voltage of varactors. We can tune the center frequency of doubler from 8.7GHz to 11GHz by changing the bias voltage from 0.2V to -0.2V. Moreover, we also measured phase noise of the output which is exactly 6dB higher than the input from 100KHz to 10MHz offset which is very close to the theoretical limit (Fig. 4.14). Each buffer consumes around 13mA of DC current with 1.4V power supply which can be easily improved using efficient design and output matching. The center frequency can be tuned using the bias voltage of varactors. Fig. 4.15 shows the chip photograph of frequency doubler. Table 4.1 shows the comparison between various works. Here, [27] and [28] do not employ any output buffer. The conversion loss of this doubler is the lowest among passive CMOS doublers reported

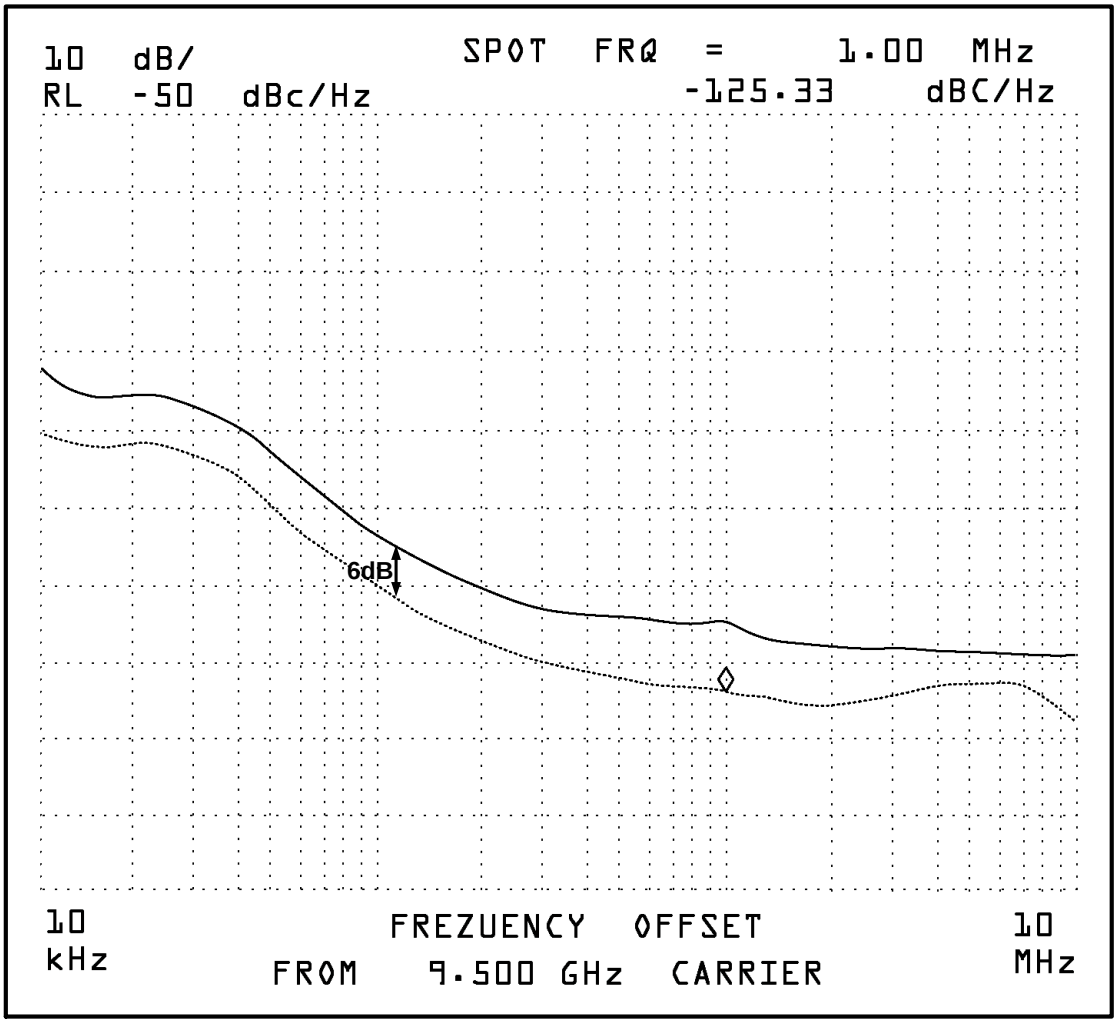

Figure 4.14: Measured phase noise

so far. The injection locked system are limited by the locking range and they do not work outside the locking range. However, passive structures always operate though the conversion loss increases as the frequency shifts.

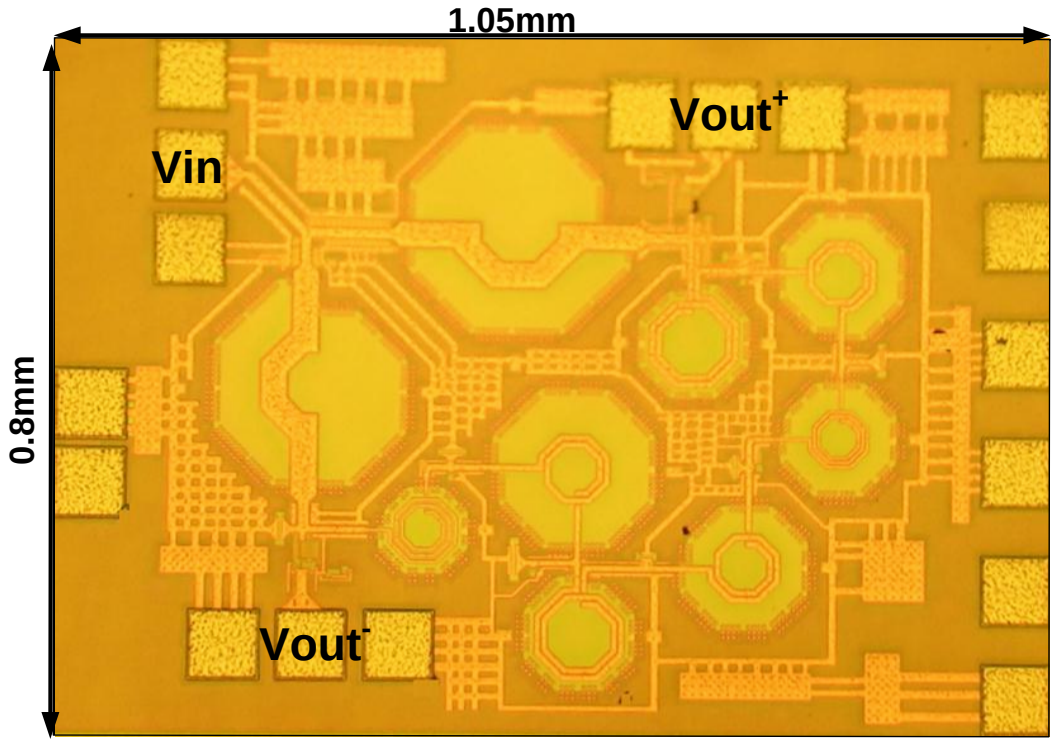

Figure 4.15: Chip photograph

Table 4.1: Comparison with prior art

Ref.	**Center Freq.**	**Conv. Gain**	**Core PDC**	**Locking Range/ Bandwidth**	**Input**	**Output**
[25]	13GHz	4dB	5.2mW	30%	Differential	Differential
[26]	16.2GHz	-	22mW	19%	Polyphase	Polyphase
[27]	11GHz	-15dB	0	Broadband	single	single
[27]	3GHz	-10dB	0	Broadband	single	single
[28]	40GHz	-5	132mW	Broadband	single	single
This work	20GHz	-3.4dB	0	Broadband	single	Differential

4.4 Design and Measurement of Frequency Tripler

4.4.1 A standing wave resonator design

As mentioned earlier, harmonics higher than 2^{nd} present themselves with multiple challenges. Frequency tripler requires an additional level of phase matching in case of indirect conversion as fundamental frequency has to be phase matched with 2^{nd} as well as 3^{rd} harmonic. Along with phase matching, one has to ensure proper isolation between various harmonics. With these requirements in consideration, we come up with a symetric standing wave resonator for frequency tripler as shown in Fig. 4.16. The resonator consists of two nonlinear propagating path each made up of two sections of a bandgap structure. For appropriate phase matching, phase shifts per section of fundamental, 2^{nd} and 3^{rd} harmonic are $\pi/2$, π and $3\pi/2$ respectively. This implies, 1^{st} and 3^{rd} harmonics are placed in 1^{st} and 2^{nd} passband respectively. The 2^{nd} harmonic lies in the stopband.

For better isolation, input is desired to be differential. The differential input produces in-phase 2^{nd} but differential 3^{rd} harmonic. Hence, the differential output from the resonator does not contain any second harmonic. The half circuits for both differential and in-phase situations are also presented in Fig. 4.16.

4.4.2 Implementation

In order to implement the resonator, we need a balun to provide differential input and buffers to probe output. The schematic of the proposed resonator is shown in Fig. 4.17. We chose center frequency to be close to 100GHz and a 130nm CMOS process for the implementation of frequency tripler. The peak measured f_{max} of a 130nm CMOS process

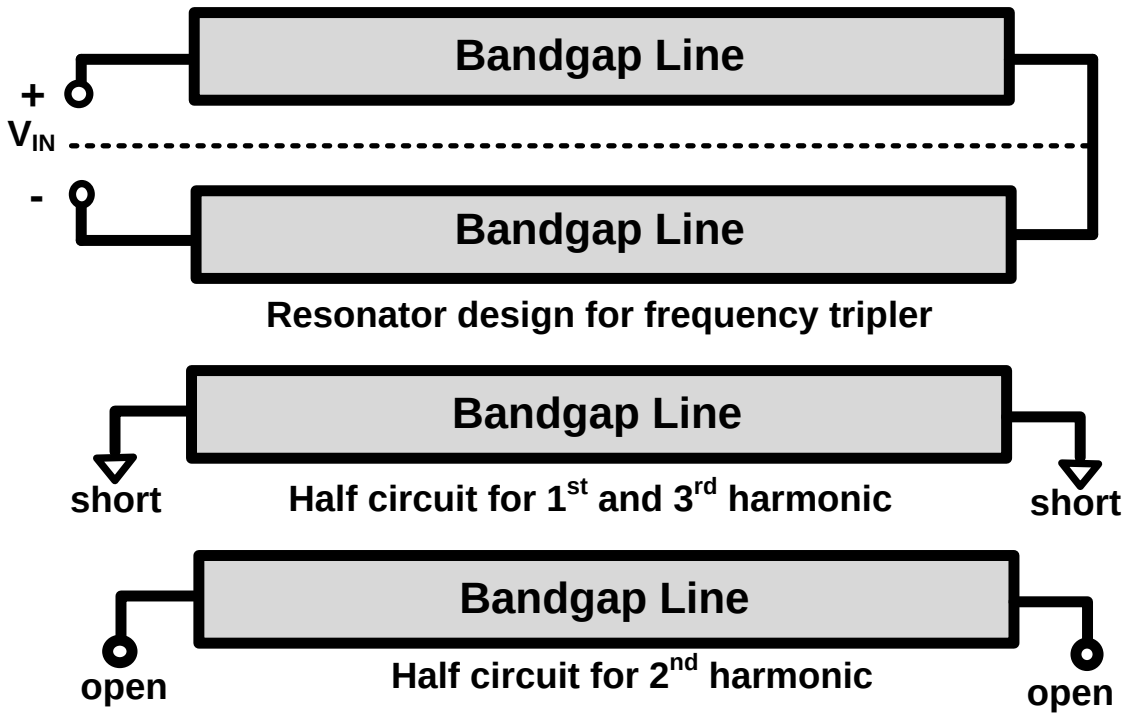

Figure 4.16: Resonator design for frequency tripler

is around 135GHz [29], hence we are operating very close to f_{max} of the process.

Fig. 4.17 shows implementation of resonator using transmission lines loaded with varactor. All the lines are implemented as coplanar transmission lines with ground shielding. The 4μm thick top metal provided by this process is used for the signal line and bottom metal is used as ground shielding. The dimensions of transmission lines are shown in Fig. 4.17. The distance between signal and ground planes are shown in Fig. 4.18.

The tripler requires a broadband balun from 30-38GHz to feed differential inputs to the resonator. The passive implementation of balun is appropriate for broadband operation with superior amplitude and phase imbalance however passive balun at desired frequecies can be very bulky. For smaller chip size, we use common gate and common

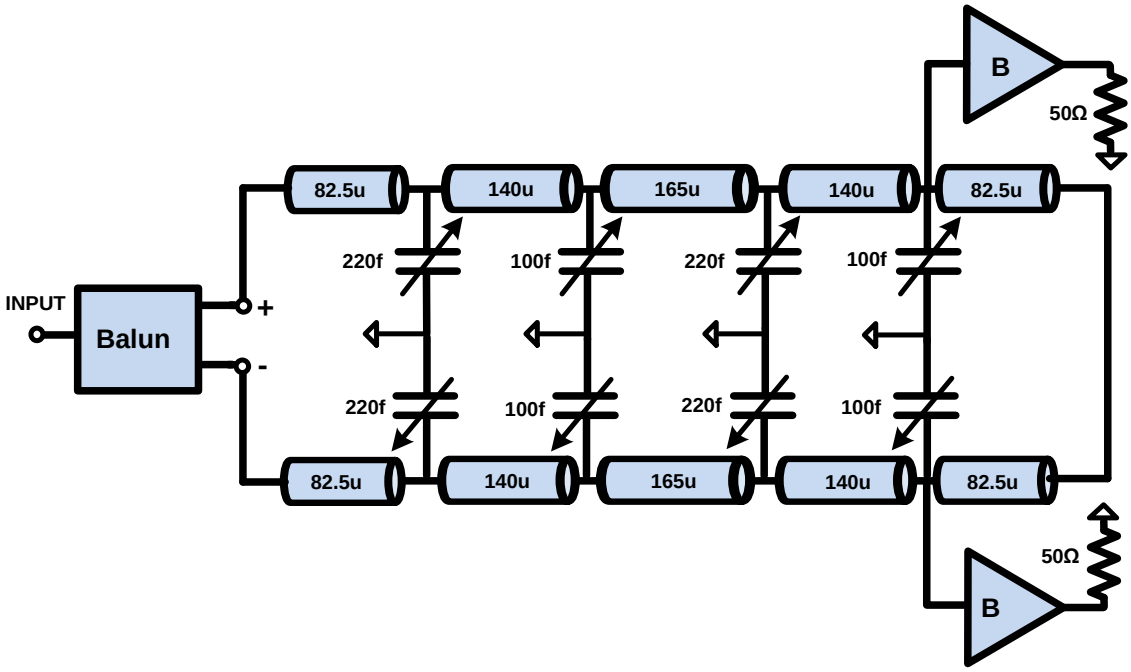

Figure 4.17: Schematic of frequency tripler

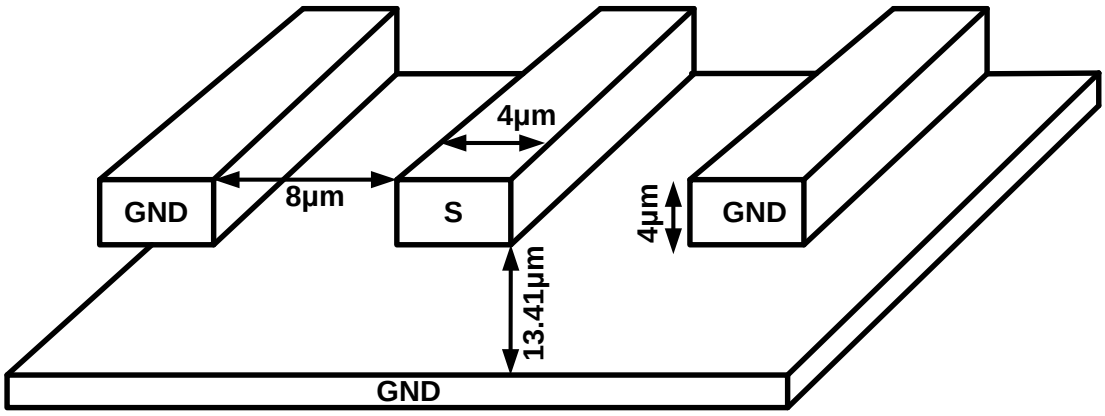

Figure 4.18: Metal layers and dimension of transmission lines.

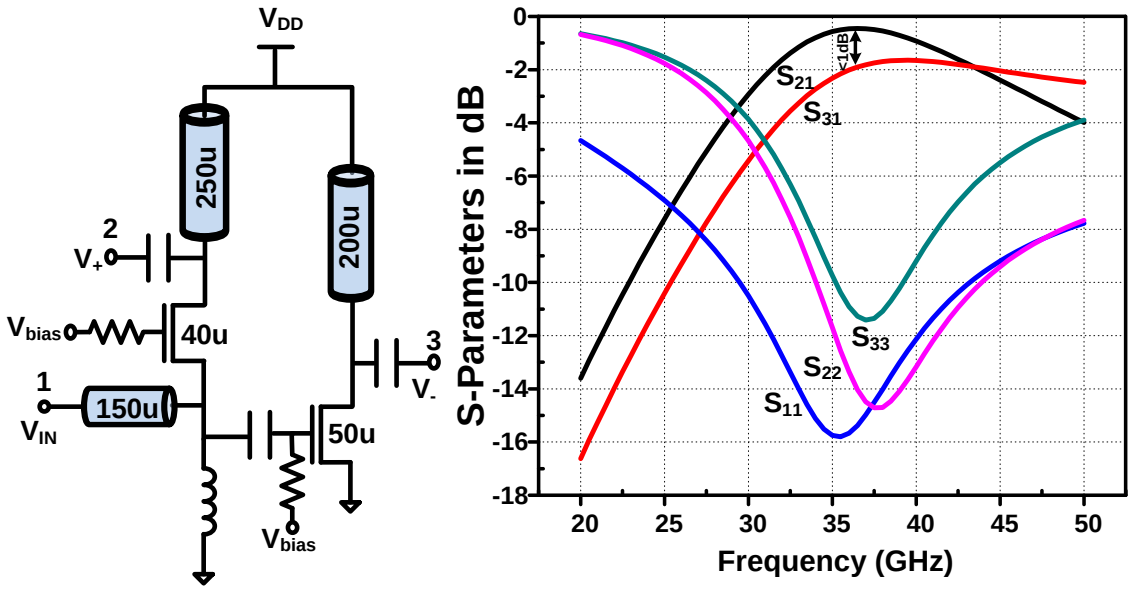

Figure 4.19: Schematic of balun

source stages to generate both inverting and non-inverting outputs simultaneously [30]. The specific topology offers broadband operating because of common gate topology at the input. The balun is shown in Fig. 4.19. The simulated phase error of balun is shown in Fig. 4.20. The phase error in the desired range of frequencies is less than 2^o

The gains of both stages are adjusted to achieve minimum amplitude imbalance at the output. The inductors are implemented using transmission lines as it helps in placement of balun layout with other components in a more symetrical way. Fig. 4.19 shows the large signal S parameter simulation results. The amplitude imbalance is less than 1dB and broadband input matching is achieved simultaneously.

The design of buffers is particularly challenging as we desire to probe very high frequency. The differential measurement is not possible at these frequencies hence measurements are performed single endedly. This implies, buffers should be able to isolate the resonator from the landing effect of probe. At the same time, buffer should have

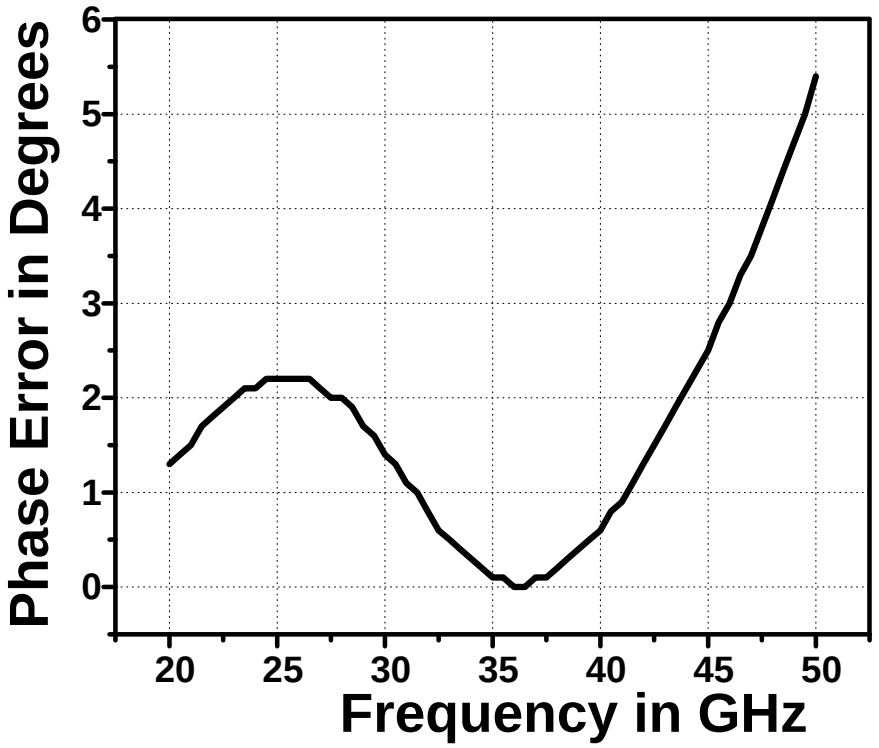

Figure 4.20: Phase error of balun.

minimum loading effect on the resonator itself so that it does not effect the operation of resonator itself. Owing to these requirements, we choose tapered buffer design. The schematic of buffer is shown in Fig. 4.21. The output pad is designed to become the part of output matching network. The large signal return loss is also shown in Fig. 4.21.

The input insertion loss is shown in Fig. 4.22. The broadband input matching is because of the balun topology. Fig. 4.23 shows conversion loss and output power against various input powers. The best conversion loss we achieve is around 12dB.

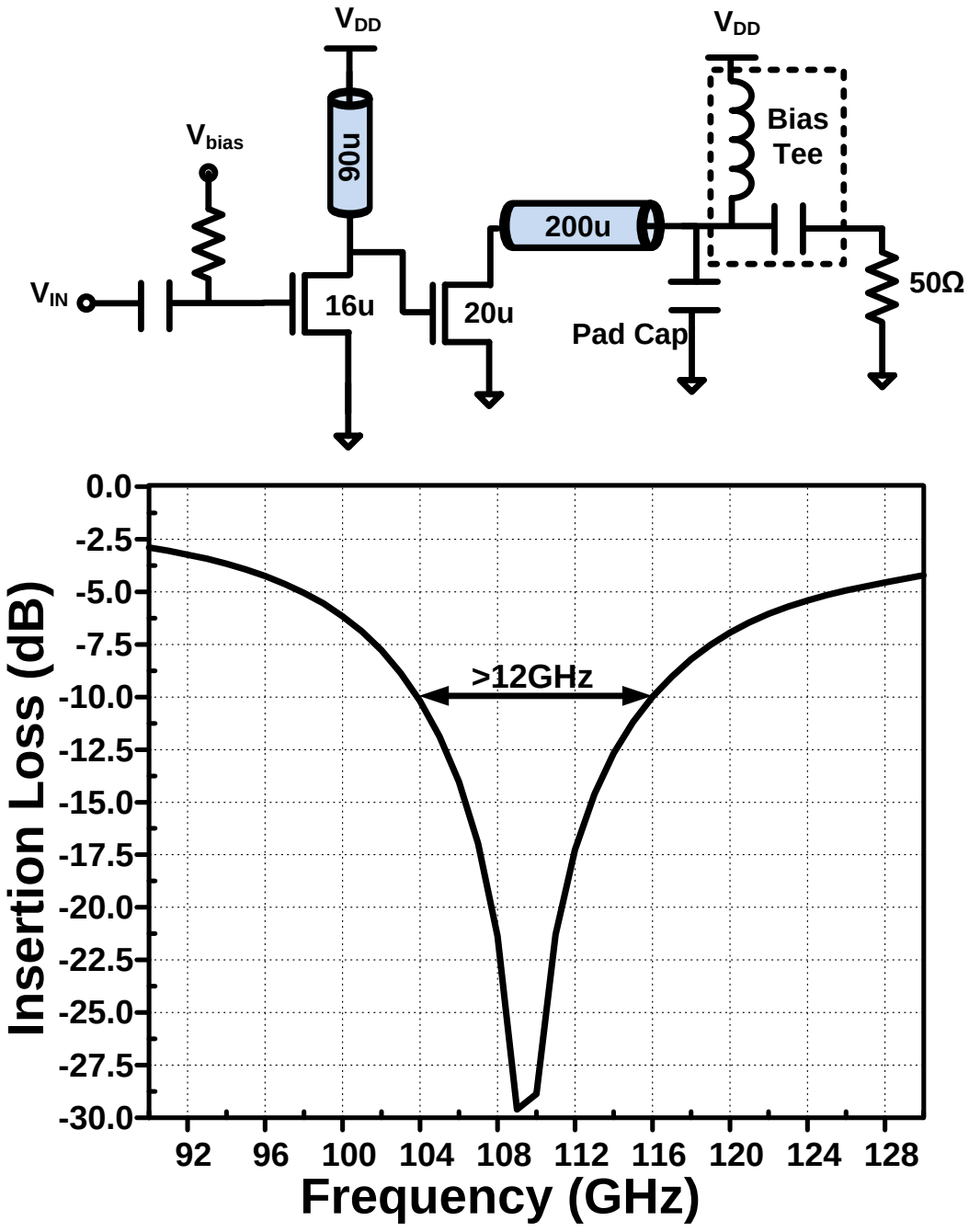

Figure 4.21: Schematic of output buffer.

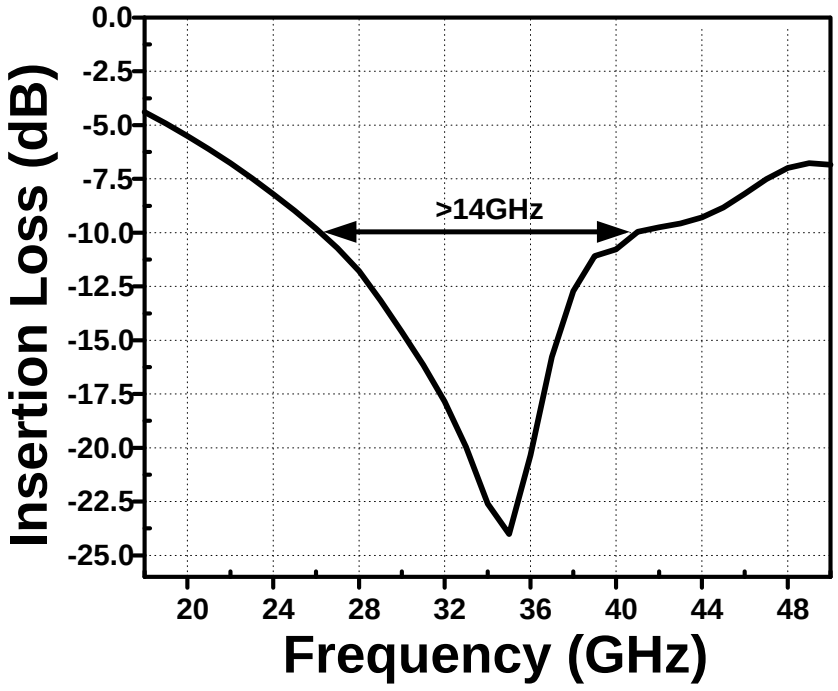

Figure 4.22: Insertion loss of frequency tripler.

4.4.3 Measurement results

Fig. 4.24 shows the chip picture. In order to perform measurements chip was mounted on the PCB and all the DC pads were wirebonded. Fig. 4.25 shows the measurement setup used to determine output frequency and power. The output is measured using a WR-08 probe by GGB with a built-in bias-T. The loss of probe is measured using a 110GHz network analyzer to be around 2-2.5dB at frequencies from 90GHz to 130GHz. The second stage of the buffer is power up using the probe bias-T. The probe is directly attached to an OML harmonic mixer via a WR-08 waveguide. An external diplexer is employed to connect to a spectrum analyzer and signal generator. The conversion loss of harmonic mixer is measured at various LO powers for 8_{th}, 10_{th} and 12_{th} harmonic using a PM4 calorimeter. The loss of mixer is around 42dB around frequencies of interest.

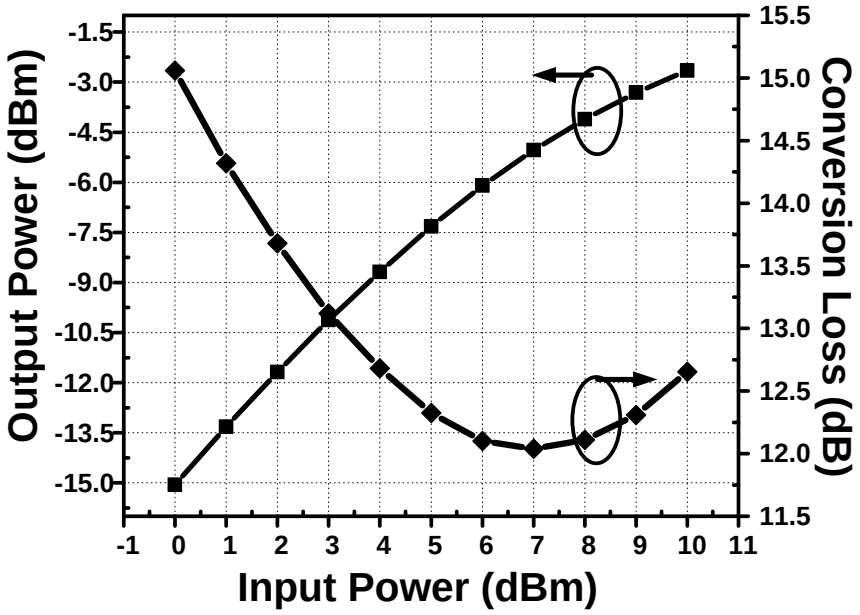

Figure 4.23: Simulated conversion loss of frequency tripler.

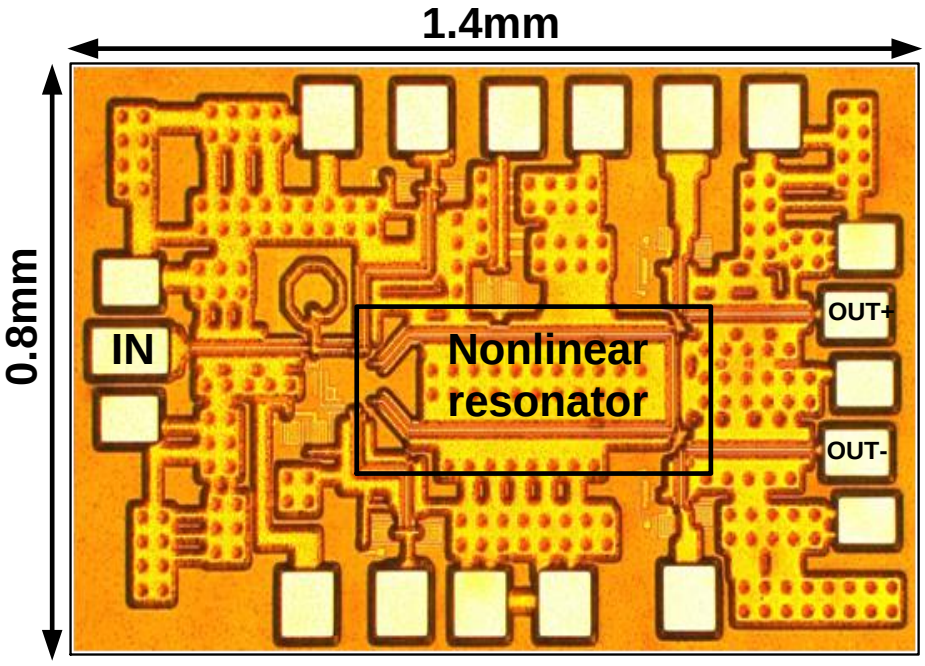

Figure 4.24: Chip photograph of frequency tripler

Table 4.2: Comparison with prior art

Ref.	**Process.**	**Frequency**	**P_{DC} (mW)**	**P_{out} (dBm)**	**DC-RF (%)**	**Conv. gain**	**Bandwidth/Locking range**
MTT-2012 [31]	0.18μ SiGe	96GHz	75	-7	0.3	-7	5.5%
IMS-2010 [32]	65nm CMOS	93GHz	19.8	-7	1	-7	6%
JSSC-2008 [33]	90nm CMOS	60GHz	23.8	-27	0.01	-27	13.3%
MTT-2011 [34]	0.15μ pHEMT	60GHz	56	-2.6	0.89	-1.6	10.5%
This Work	130nm CMOS	98GHz	135	-1.5	0.6	-12.2	11.34% (3-dB)

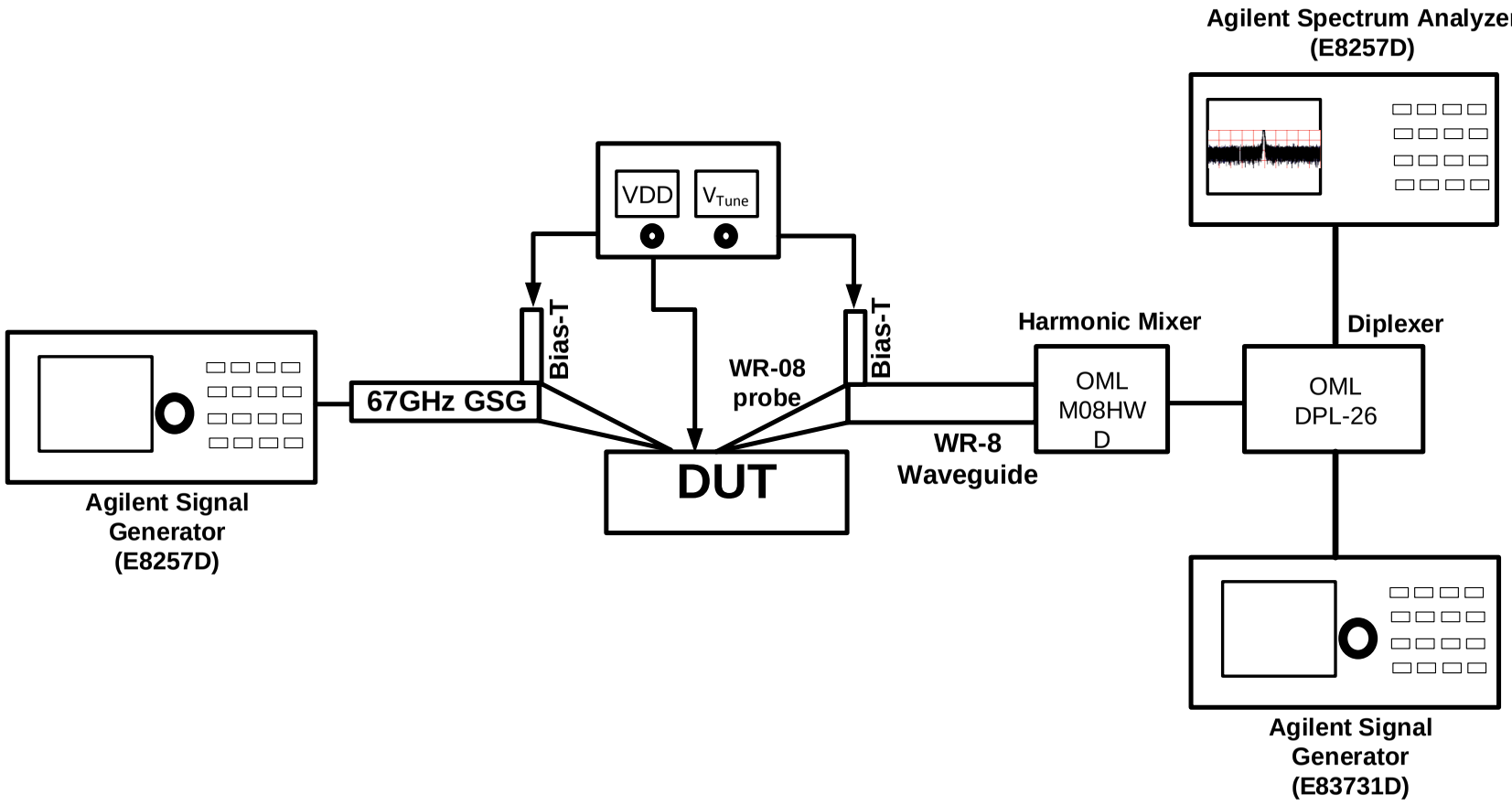

Figure 4.25: Measurement Setup

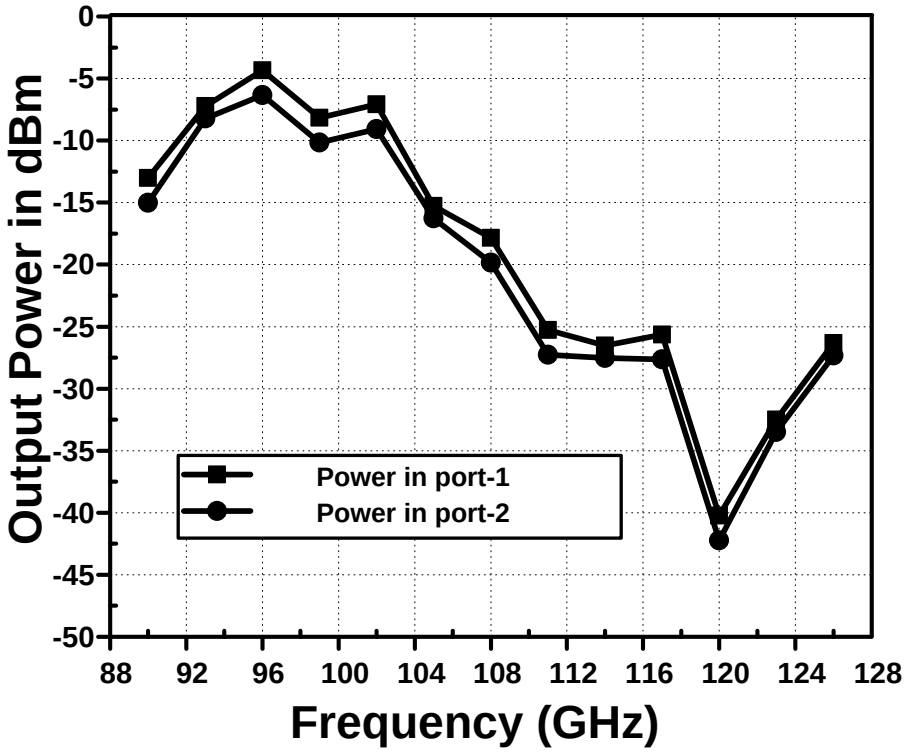

Figure 4.26: Measured amplitude imbalance between two ports

We performed the measurments at both output ports. Fig. 4.26 shows the measured amplitude imbalance between both outputs. The measured difference is around 1dB from 90GHz to 126GHz. Fig. 4.27 shows the measured conversion loss and output power against various input powers at 96GHz. The best conversion loss achieved is around 12.3dB. Fig. 4.28 shows the measured output power against frequency for different bias voltages across varactor. The 3dB bandwidth is around 11.2Ghz. Fig. 4.29 shows the measured LO spectrum at 100GHz.

Table 4.2 compares our work with the state of art. All the works in table 4.2 are developed in better processes including pHEMT and SiGe. Our proposed topology achieves higest power with comparable bandwidth.

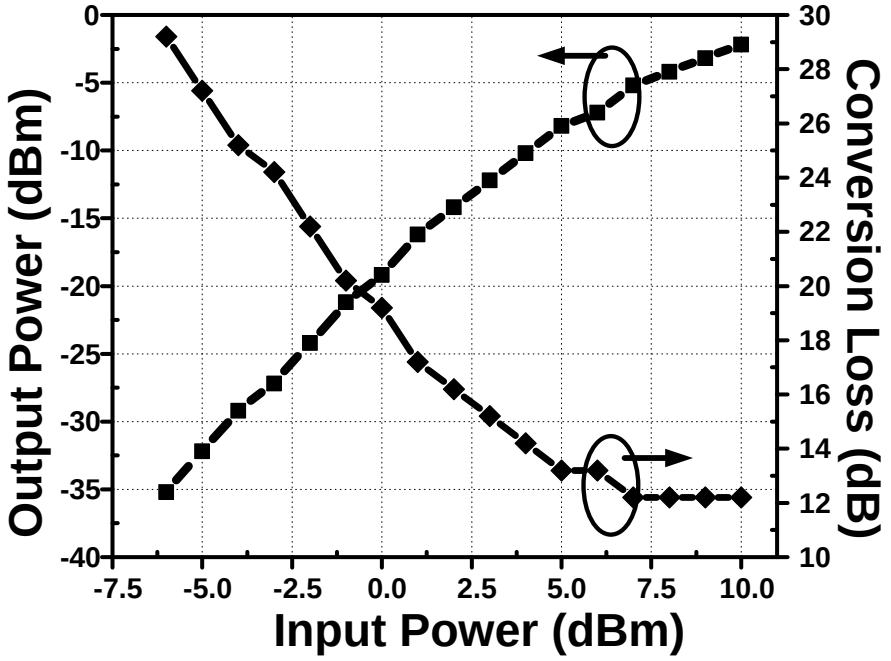

Figure 4.27: Measured conversion loss and output power against input power

4.5 Conclusion

In this work, we focus on nonlinear transmission lines (NLTLs) based frequency multipliers. Two methodologies are developed to go beyond the limitations of multipliers: i) we used bandgap structure to resolve dispersion which is inherently present in any discrete wave propagating structure. ii) in order to enhance conversion loss performance and relax input power requirement, we employ a resonator approach in combination with active loading. We build two prototypes: a 20GHz frequency doubler is implemented in a 65nm process as a proof of concept, second to show the feasibility of our approach near f_{max}, a 100GHz frequency tripler is implemented in a 130nm process. The achieved conversion loss is 3.5dB for doubler and 12.2dB in case of tripler. Both structures take single ended input and generate differential output. The frequency tripler can generate maximum power of about -1.5dBm. The relative bandwidth of doubler and tripler is

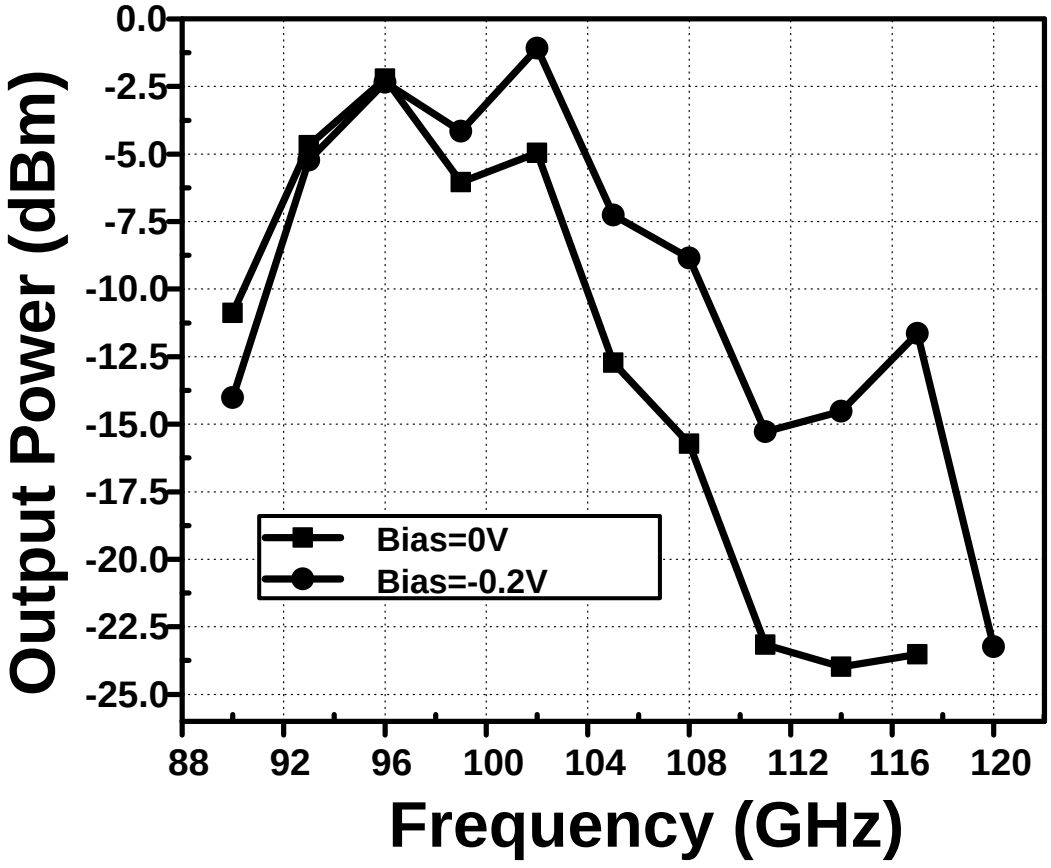

Figure 4.28: Measured output power for various bias points

about 23% and 12.3%. The frequency tripler outperforms any previously reported work in terms of output power and 3dB bandwidth at the same technology node.

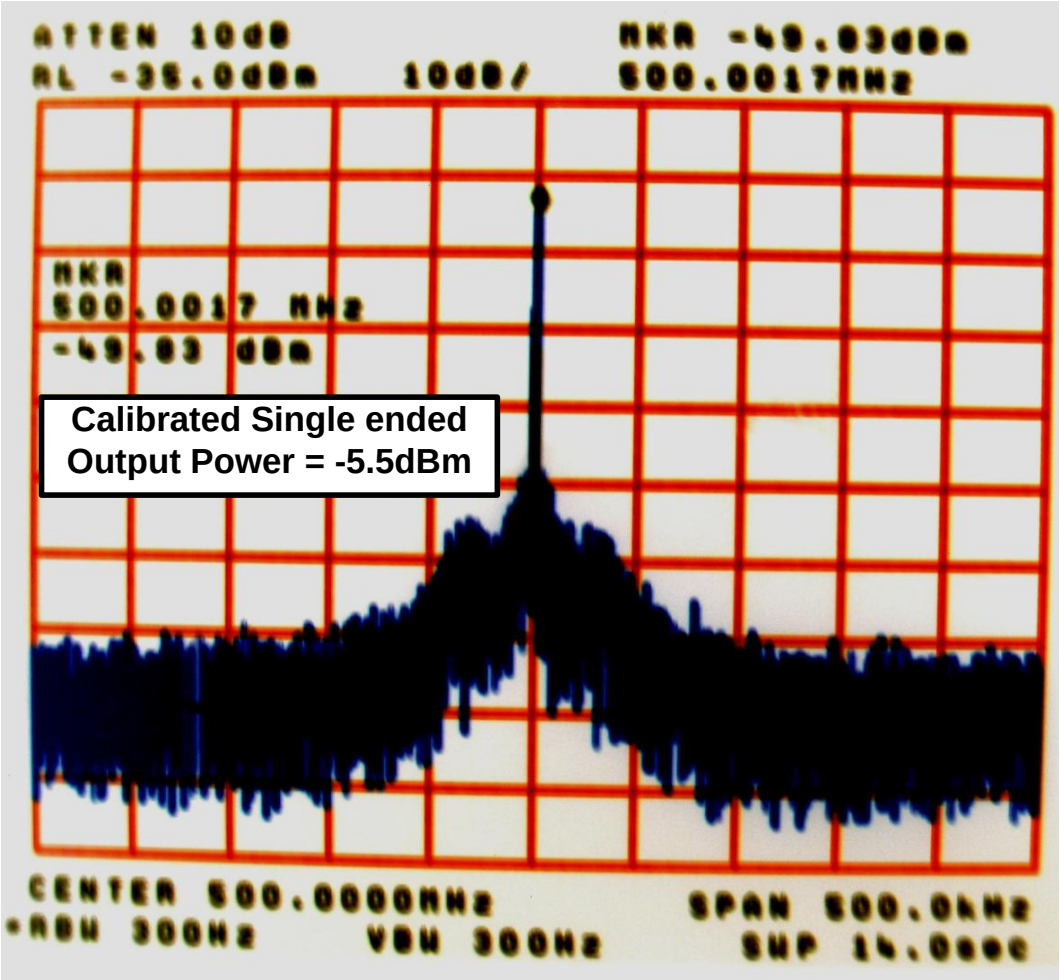

Figure 4.29: Single ended measured spectrum

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